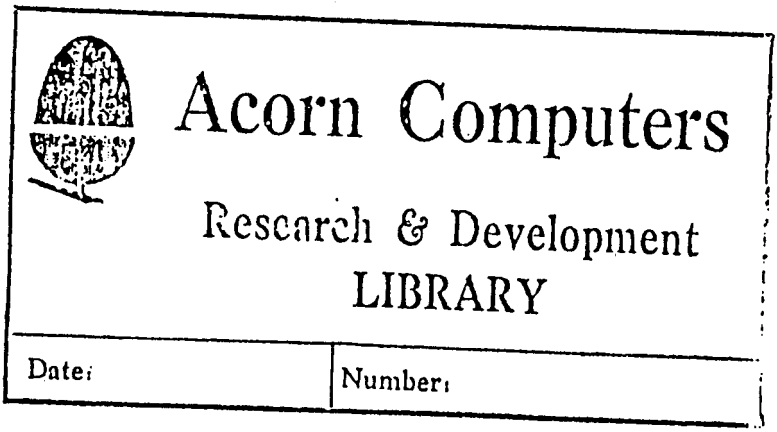
A500 Hardware Guide

Part No *???,???*
Issue No 0.0
10 November 1916
draft • not for publication

INSIDE FRONT COVER



ISBN ? ????? ??? ?

Published by:
Acorn Computers Limited, Fulbourn Road, Cherry Hinton, Cambridge CB1 4JN, UK

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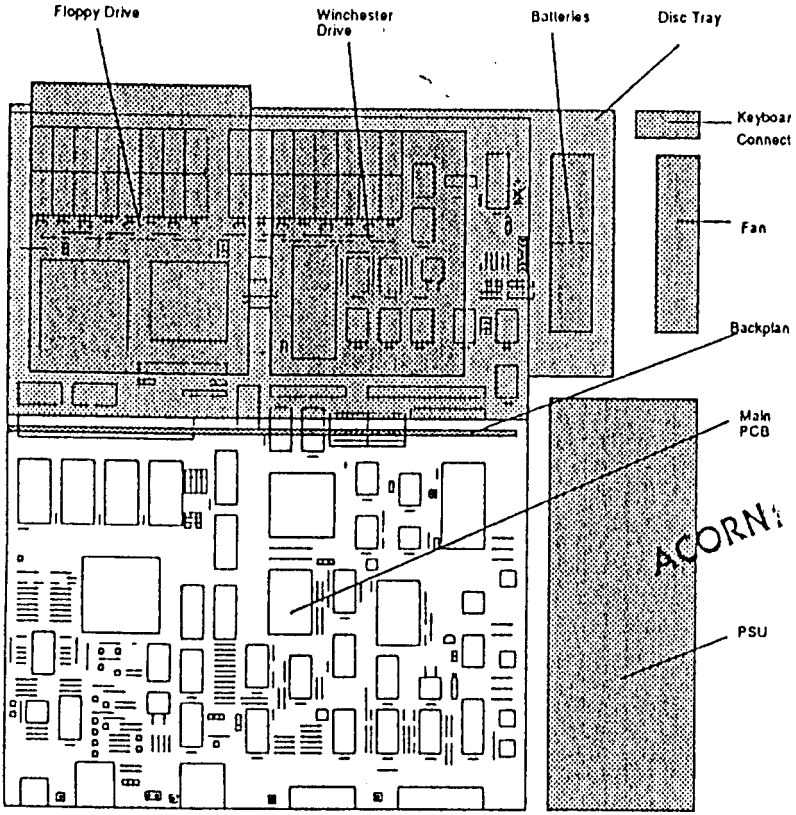
Floppy Drive
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1. Introduction

The A500 is a high performance personal workstation intended for software development of future Acorn products. It is built around four fully custom VLSI devices. These are the A Series chip set, which comprise the Acorn Risc Machine (ARM), Memory Controller (MEMC), Video Controller (VIDC) and Input Output Controller (IOC). With the addition of a number of peripheral chips. a Case, a PSU, a detachable keyboard and a CRT the A Series chip set is the basis of a flexible computing engine.

See ARM,MEMC,VIDC and IOC datasheets for additional information on the A series chip set.

FEATURES

- 8 MIPS peak
- 4 MByte RAM
- 1/4 MByte ROM
- Virtual Memory support
- 95 key keyboard with speaker and mouse
- 1.6 MByte floppy disk
- 20 MByte winchester disk
- Parallel printer interface
- ECOnet interface
- RS423 serial interface
- Four internal IO expansion slots
- Battery backed-up Real Time Clock and 256 Bytes of RAM
- Linear RGB output
- Composite video output
- High quality stereo sound output
- 1152 x 864 at 1 bit per pixel 60 Hz refresh
- 640 x 480 at 4 hits per pixel 60 He refresh
- 640 x 256 at 8 bits per pixel 50 Hz refresh

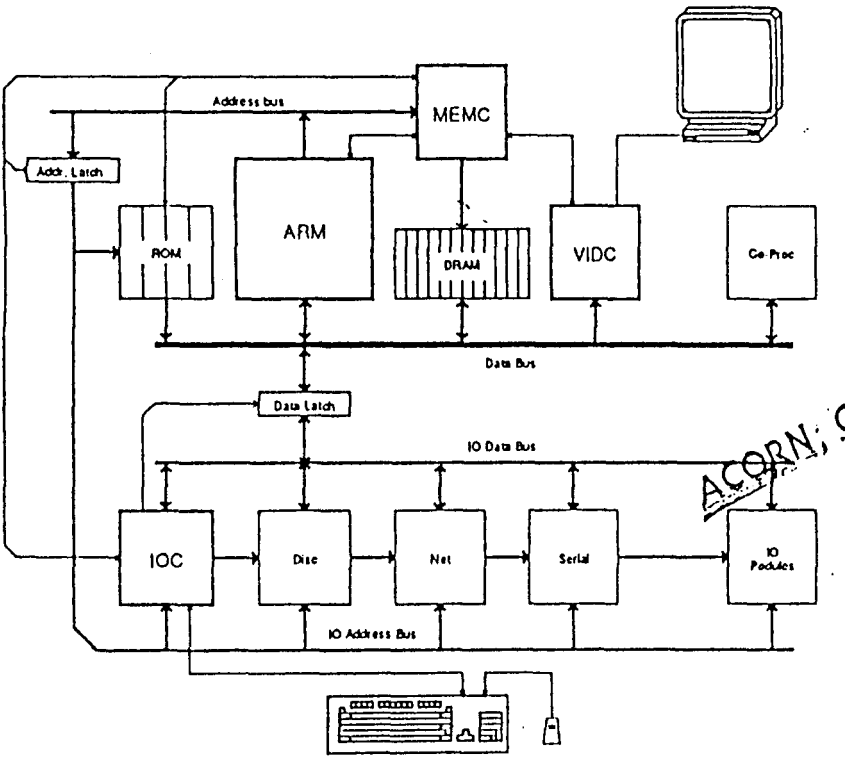


Figure 1: A500

2. General Circuit Description

The ARM is a low cost, pipelined 32 bit reduced instruction set processor with very low interrupt latency. It accepts instructions and manipulates data via a high speed 32 bit data bus and 26 bit address bus. All instructions are restartable allowing true virtual mcmory support.

The Memory Controller (MEMC) acts as the interface between the ARM and the rest of the *A Series* chip set, Read-Only memories (ROM), and Dynamic memory devices (DRAM), providing all the critical system timing signals.

Up to 4MBytes of DRAM may be connected to MEMC, which provides all signals and refresh operations for a wide variety of standard DRAMs. A *Logical to Physical Address Translator* maps the Physical Memory into a 32MByte Logical address space (with three levels of protection) allowing Virtual Memory and Multi-Tasking operations to be implemented. Fast "page mode" DRAM accesses are used to maximise memory bandwidth. The. VIDC requests data from the RAM when required, and buffers it in one of three FlFOs before using it. Data is requested in blocks of four 32-bit words, allowing efficient use of paged-mode DRAM without locking up the system data bus for long periods.

MEMC supports Direct Memory Access (DMA) read operations with a set of programmable *DMA Address Generators*, which provide a circular buffer for Video data, a linear buffer for Cursor data, and a double buffer for Sound data.

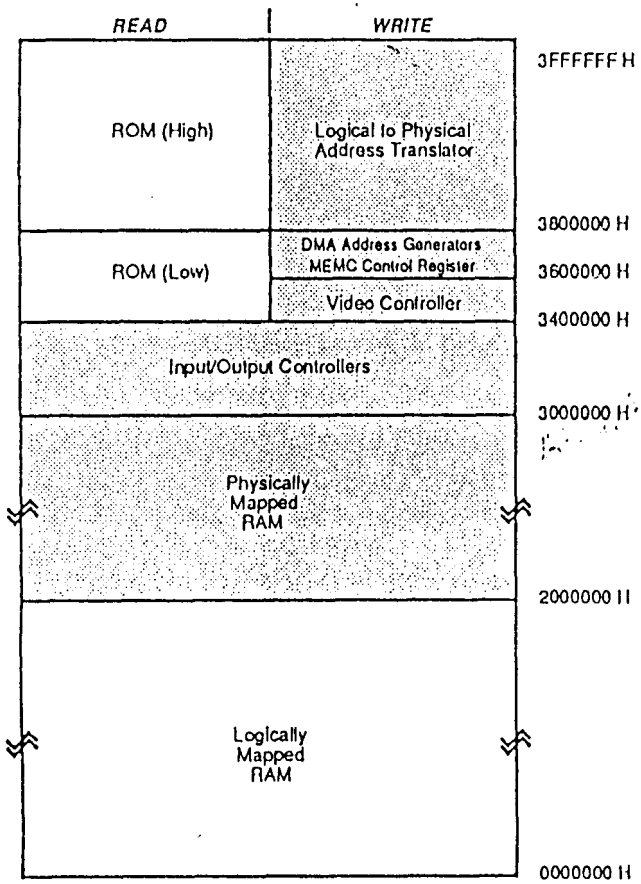
The Video Controller (VIDC) takes video data from the video FIFO, serialises it and passes it through a colour look-up palette, and converts it to analogue signals for driving the CRT guns. The chip also controls all the display timing parameters and controls the position and pattern of the cursor sprite. In addition, the VIDC incorporates an exponential Digital to Analog Converter (DAC) and stereo image table for the generation of high quality sound from data in the DRAM.

The VIDC is a highly programmable device, offering a very wide choice of display formats. The pixel rate can be selected between 8 and 24MHz and the data can be serialised to either 8, 4, 2, or 1 bit per pixel. The horizontal timing parameters can be controlled to units of 2 pixels, and the vertical timing parameters can be controlled to units of a raster. The colour look-up palette which drives the three on-chip DACs is 13 bits wide, offering a choice from 4096 colours or an external video source.

The cursor sprite is 32 pixels wide, and any number of rasters high. Three simultaneous colours (again from a choice of 4096) arc supported, and any pixel can be defined as transparent, making possible cursors of many shapes. It can be positioned anywhere on the screen. The sound system implemented on the device can support up to 8 channels, each with a separate stereo position.

3. The Memory sytem

All data is manipulated through internal registers, memory or the co-processor interface which is only supported by the 2 µ ARM. The memory consists of physical ram and memory mapped devices. These devices are the programming registers of the MEMC, VIDC. IOC and the IO peripherals. The partitioning of the memory space is shown in figure 2. The shadded areas are accessible only when the ARM is in supervisor mode.



4. The Video system

The VIDC is reponsible for all the system display functions and only a minimal amount of off-chip line driving is required to drive a standard monitor, which may be monochrome or colour, and may support PAL broadcast standard timings or, for higher resolutions, a 32 kHz line rate.

The A500 also supports a 1152*864 resolution monochrome mode, which exploits the VIDC external high-resolution shifter to give a 96 MHz pixel rate. A suitable monitor for this display mode would have a 60 kHz line rate.

5. The Sound system

The sound system is based on the VIDC stero sound hardware, External analogue anti-alias filters are used which are optimised for a 20 kHz sample rate. The high quality sound output is available at a 3.5mm stero jack socket at the rear of the machine which will directly drive personal stereo headphones or alternately an amplifier and speakers. A mono mix of the sound output is sent to the keyboard loudspeaker. In addition various mixing and muting functions are provided.

5.1 The Video Controller Sound System Hardware

VIDC contains an independent sound channel consisting of the following components. A four-word FIFO buffers sixteen 8-bit sound samples with a DMA request issued whenever the last byte is consumed from the FIFO. The sample bytes are read out at a constant sample rate programmed into the 8-bit Audio Frequency Register; this may be programmed to allow samples to be synchronously output at any integer value between 3 and 255 microsecond intervals (with an 24MHz VIDC clock).

The sample data bytes are treated as sign plus seven-bit logarithmic magnitude and after exponential digital to analogue conversion, de-glitching and sign-bit steering are output as a current at one of the audio output pins to be integrated and filtered externally.

VIDC also contains a bank of eight stereo image position registers each of 3 bits. These 8 registers are sequenced through at the sample rate with the first register synchronised to the first byte clocked out of the FIFO. Every sample time is divided into eight time slots and the three bit image value programmed for each register is used to pulse width modulate the output amplitude between the LEFT and RIGHT audio current outputs in multiples of time slot subdivisions. This allows the signal to be spatially positioned in one of seven stereo image positions. (The first period of every sample is muted internally to absorb any DAC output current glitches).

For further information refer to the VIDC data sheet.

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5.2 The Memory Controller Sound System Hardware

MEMC provides three internal DMA address registers to support Sound buffer output; these control the DMA operations performed following Sound DMA requests from VIDC. The registers allow the physical addresses for the START, PNTR (incremental) and END buffer pointers to a block of data samples in the lowest half Megabyte of physical RAM to be accessed and operate as follows: programming a 19-bit address into the PNTR register sets the physical address from which sequential DMA reads will occur (in multiples of 4 words) and programming the END pointer sets the last physical address of the buffer. Whenever the PNTR register increments up to this END value the address programmed into the START register is automatically written into the PNTR register for the DMA to continue with a new sample buffer in memory. A Sound Buffer Interrupt (SIRQ) signal is generated when the reload operation occurs which is. processed by IOC as a maskable interrupt (IRQ) source.

The Memory Controller also includes a sound channel enable signal which is necessary in order to disable the sound DMA acknowledgments to the Video Controller when the sound output is to be suppressed. Because this enable/disable control signal is not synchronised to the sound sampling requests one would normally only disable requests after the waveforms being synthesised have been programmed to decay to zero amplitude; the last value loaded into the Audio data latch in the VIDC will in fact be output to each of the Stereo image positions at the current Audio Sample rate.

There are several important constraints which must be observed when programming the Sound DMA Buffer addresses. Firstly, because a 4-word FIFO is provided in VIDC, buffer lengths are constrained to multiples

of four words: although 17 bits in the address registers are programmable, the two low-order bits are ignored. Secondly, the END condition test is in fact a test for equivalence rather than 'greater-than-or-equal', with the result that the END address must be programmed to an address greater than the (dynamically incrementing) PNTR register. In addition, as soon as a Buffer finished signal interrupt is detected then the new END value must be programmed because the PNTR register is now advancing from the reloaded START address - interrupt acknowledge latencies may well become critical with high sample frequencies and short DMA buffers.

The provision of the three registers is in fact well suited to both single and multiple DMA buffer systems. In the case of a simple waveshape that is to be repeatedly output then the START and END registers can be left programmed to point to the physical buffer addresses and the PNTR address will automatically loop round with no further action required. With two or more buffer operation the reprogramming of the END of the current buffer and the START of the next buffer are the only critical operations and should be performed together as soon as possible after a hardware buffer pointer switch interrupt has occurred.

5.3 The I/O Controller Sound System Hardware

IOC provides three programmed output control signals which are to turn on or off external analogue switches in order to provide routing of the audio signals, as well as an interrupt enable/status/reset register interface for the Sound Start Buffer reload signal generated by the Memory Controller.

Bit 1 in the Interrupt High Register bank has been allocated in IOC and the interrupt may be enabled by setting this bit in the INTmask High register, monitored directly in the INTstatus High register and masked with the current enable mask in the INTrequest High register, and cleared by writing to this bit in the INTclear register.

The three audio routing control lines are defined as OMUTE which disables sound output from the Podule Analogue Output bus, PMUTE which disables external Podule Analogue Input signals being mixed with the internal sound source, and SMUTE which mutes all output to the internal loudspeaker situated in the keyboard. The OMUTE and PMUTE reflect the status of bits 14 and 13 respectively of the programmable (write-only) External Register (which are uninitialsed at power up) and SMUTE which reflects the state of Bit 5 of the Control port of IOC (the Internal speaker is muted at power up).

The stereo output to the Hi-Fi stereo output is in fact not mutable with SMUTE and always reflects the current output of the DAC channels.

6. The IO system

The IO system is controlled by the IO Controller IOC and the Memory Controller MEMC . It has a 16 bit Data interface which could be expanded to 32 bits or shrunk to 8 bits on future A Series products. The IO Bus supports all the internal peripherals and the PODULE expansions.

6.1 Programming Model

The Bank B[0:2], Type T[0:1], Chip Select CS and Addresses Lines A[2:6] of IOC are joined to the CPU address lines and the IOC and peripherals are viewed as memory mapped devices. This allows the programmer to specify in a single memory instruction the peripheral to be accessed and the type of timing cycle it requires. As shown in figure 2 the IO Controller space is divided into two halves. The upper half is occupied by IOC, and the lower half is left for additional IO Controllers.

The IOC space is decoded into eight banks, bank zero through seven, by the B[0:2] lines. The bottom bank, bank zero, maps to the internal registers of IOC. The remaining seven banks map to the seven peripheral select lines S[1:7] respectively. The seven peripheral banks are each further decoded into four types of peripheral access by the T[0:1] lines. (See figure 2.) The type of the peripheral access determines the timing of the data transfer cycle.

A particular peripheral device may be accessed by choosing an address where CS is HIGH, B[0:2] decodes to the appropriate peripheral select, and T[1:0] selects a cycle with timing to suit the accessed device. The remaining low order address lines may be used to select the register within the device.

6.2 Access Speed

While the peripherals appear as memory mapped devices, it is not possible for accesses to them to be completed in the same time as accesses to main memory. Four different access cycle timings are available and the timing for an access is determined from the state of T[0:1] at the start of the access.

6.2.1 Byte Accesses

To access byte wide peripherals byte instructions should be used. A byte store operation will place the written byte on all four bytes of the word and will therefore correctly place the desired value on the lowest byte of the IO Bus. A byte or word load may be used to read a byte wide peripheral into the lowest byte of an ARM register.

6.2.2 Half-Word Accesses

To access half-word peripherals word instructions should be used. When storing, The half-word must be placed on the upper 16 bits, D[16:31]. To maintain upwards compatibility half-word stores should replicate the written data on both half-words. When loading, the upper sixteen bits are undefined.

6.2.3 Word Accesses

These are not supported on the A500.

6.3 10 address memory mapping

The IOC is connected as detailed in table 1.

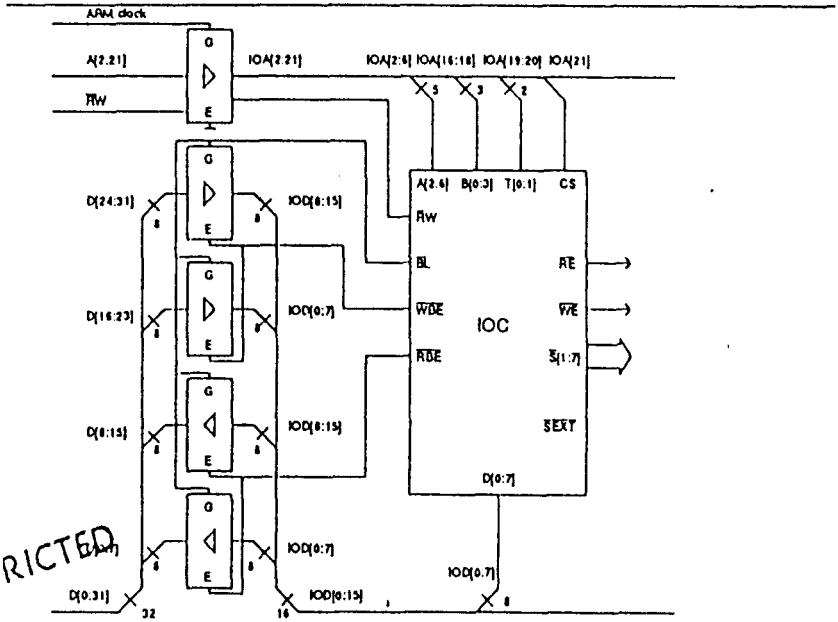


Figure 2: A500 IO system

6.4 IOC Internal Register Mal)

All internal registers are accessed with no wait states, and accesses take two REF8M cycles to complete. The internal registers are decoded as bank zero, so to access them the B[0:2] lines must all be LOW and the IOC must be selected by taking CS HIGH. The individual registers are then addressed using the A[2:6] lines. The registers are decoded on word boundaries. The state of the T[0:1] lines is ignored. The address are shown in table 2 below.

6.5 I0 peripheral memory map

The IO devices in the A500 are accessed using the addresses shown in table 3 below. External podules should only be used at the slowest speed to allow for external buffer delays.

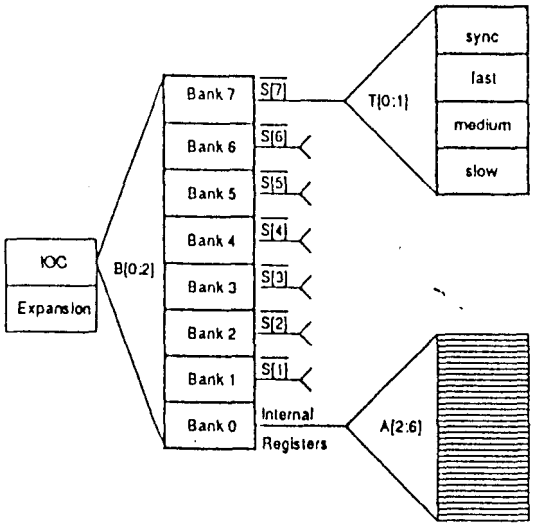


Figure 3: Decoding Structure

IOC		ARM
[OE]	=	[A[21]]
[T[1]]	=	[A[20]]
[T[0]]	=	[A[19]]
[B[2]]	=	[A[18]]
[B[1]]	=	[A[17]]
[B[0]]	=	[A[16]]

Table 1: IOC address mapping

Address	Read	Write
3200000H	Control	Control
3200004H	Serial Rx Data	Serial Tx Data
3200008H	-	-
320000CH	-	-
3200010H	IRQ status A	-
3200014H	IRQ request A	IRQ clear
3200018H	IRQ mask A	IRQ mask A
320001CH	-	-
3200020H	IRQ status B	-
3200024H	IRQ request B	-
3200028H	IRQ mask B	IRQ mask B
320002CH	-	-
3200030H	FIQ status	-
3200034H	FIQ request	-
3200038H	FIQ mask	FIQ mask
320003CH	-	-
3200040H	T0 count Low	T0 latch Low
3200044H	T0 count High	T0 latch High
3200048H	-	T0 go command
320004CH	-	T0 latch command
3200050H	T1 count Low	T1 latch Low
3200054H	T1 count High	T1 latch High
3200058H	-	T1 go command
320005CH	-	T1 latch command
3200060H	T2 count Low	T2 latch Low
3200064H	T2 count High	T2 latch High
3200068H	-	T2 go command
320006CH	-	T2 latch command
3200070H	T3 count Low	T3 latch Low
3200074H	T3 count High	T3 latch High
3200078H	-	T3 go command
320007CH	-	T3 latch command

Table 2: Internal register memory map

Cycle Type	Bank	Base Address	IC	Use
Fast	1	&3310000	9793	Floppy Disc Controller
Sync	2	&33A0000	6854	ECOnet Controller
Sync	3	&33B0000	6551	Serial Line Controller
Slow	4	&3240000	Podule	Internal Podules
Med.	4	&32C0000	Podule	Internal Podules
Fast	4	&3340000	Podule	Internal Podules
Sync	4	&33C0000	Podule	Internal Podules
Med.	5	&32D0000	HD63463	Winchester REGISTER WRITE
Med.	5	&32D0020	HD63463	Winchester REGISTER READ
Med.	5	&32D0008	HD63463	Winchester DMA READ
Med.	5	&32D0028	HD63463	Winchester DMA WRITE
Fast	5	&3350010	HC574	Printer Data
Fast	5	&3350018	HC574	Latch B
Fast	6	&3360000	HC574	Latch A
Slow	7	&3270000	Podule	External Podules

Table 3 Peripheral Addresses

7. Keyboard

The keyboard is a seperately housed unit which communcates with the main processor box via a duplex serial link. At the keyboard end the serial link is controlled by a 6500/11 microcontroller, and at the processor end by the IOC keyboard interface. The link is designed to support a number of different keyboards but it is hopped that only one will be necesary. The keyboard is powered via the serial link and the mono audio output is made available. The keyboard may also reset the main processor but keyboard should be designed so that plugging and unplugging them from the main processor does not cause a reset to occure.

The keyboard is responsible fur detecting keys states, tracking mouse movement, and sending data through the SPD (software protection device) for encription.

8. PCB general layout

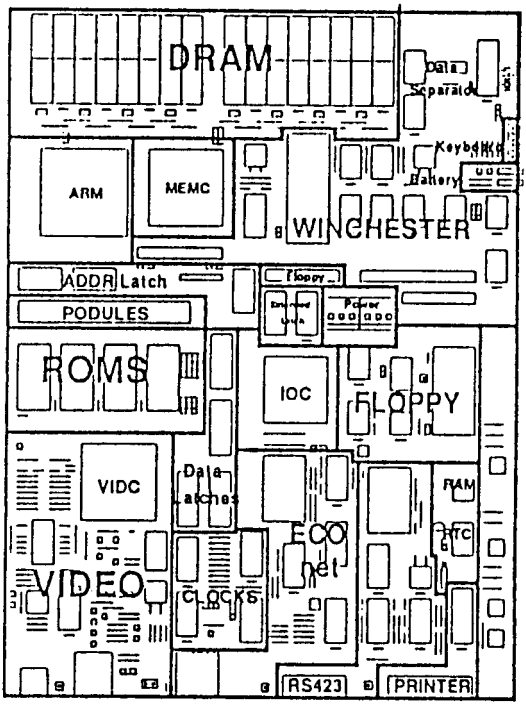


Figure 4: A500 main PCB

9. Detailed Hardware description

9.1 Physical RAM

The physical RAM consists of 32 1 MBit DRAMs. With the 8 MHz ARM the access speed must be 120 nS or better. The RAM Dout pins have series restistor (R??? to R???) to limit the slew rate and prevent undershoot. The CAS line is negated before the processor has latched data on a read cycle. The system relies on dynamic storage on the data bus to operate. 1t is important that all the loads on the data bus are CMOS-

9.2 Video

The A500 uses the VIDC custom chip. This is not compatible with VIDC2 a very similar chip which replaces VIDC. The programming differences are confined to the sound system but the video output drivers have been redesigned.

9.3 Sound

9.4 Address and Read/Write Latches

The pipelined ARM addresses and NOTread/write line are latched by IC35,IC36 and IC37 to provide valid signals thoughout both IO and ROM accesses. The latches arc controlled by the PHI2bar clock line which is stretched low during slow cycles.

9.5 Data

The ARM data but it connected to the IO data bus by a set of latches IC17,IC18,IC28,IC29. These provide two functions. Firstly they isolate the IO bus load from the main data bus and secondly they allow for the mis-match in speed between the two busses. These buffers are controlled by the BL, RBE and WBE lines from IOC . The BL line may also be driven from the backplane by an open-drain driver. When undriven the latches must remain transparent and BL is pulled high by RP1/2 and R44. The rise time of this signal must be fast enough to allow consecutive IO cycles, the limit is the output low current of BL of 10mA. The organisation of the latches is slightly unusual and is done to minimise the capacitive loading on the main memory bus.

9.6 Serial Line

The serial line is both RS232 and RS423 compatible with a typical input impedence of 5K ohms. All inputs have a 100mV offset for off-line detection. The controller is a RockweB 65C51 IC21. It has a single baud rate generator derived from its own crystal. Split baud rates are obtained by using the programmable BAUD output from IOC. The series resister R81 is needed as on reset 1C21/5 becomes an ouytput and clashes with BAUD . To allow external modems to be used the serial interface connector provides a *Ring Indicate* input which may generate an interrupt. To enable the serial interface CTS, DCD and DSR must be active. This can be achieved by connecting them to the DTR output.

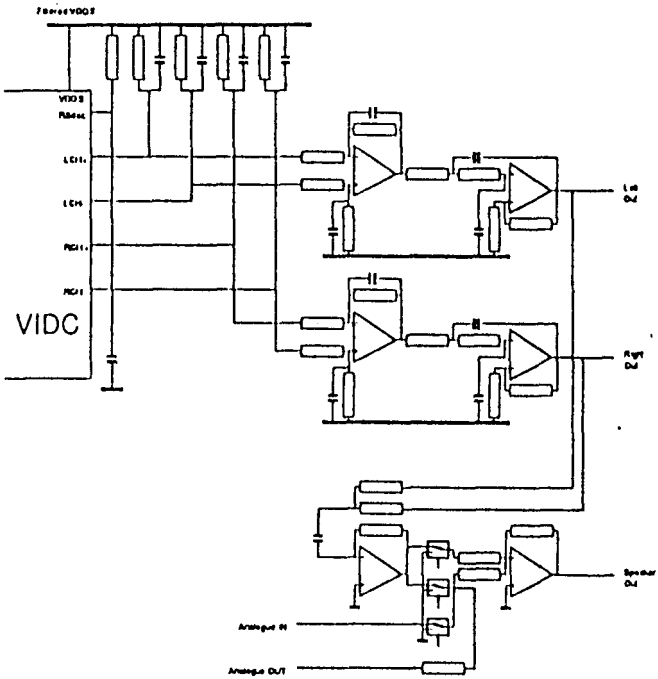


Figure 5: Sound Hardware

9.7 I2C, Real Time Clock and RAM

A Real Time Clock (RTC), 1C22 and 256 bytes of CMOS RAM, 1C23 arc provided on an I2C serial bus. Data is maintained while the mains power to the machine is switched off by two dry cells. They may be replaced while the macine is switched on without loss of data. D11 and D12 "mix" the computer and battery rails. C29 protects Vd as the machine is switched on and off. The lowest battery voltage less the voltage drop across D11 must be greater than 1.1 volts. The RTC can detect if both the mains and battery power have failed. The RAM contents should be protected with a software checksum. The RTC chip only provides a readable output pin toggled every second for fine resolution. Care must be taken to ensure monotonic time is returned to the user. (Future machines may use a combined RTC and RAM chip, PCF8583, which is currently unavailable but solves this problem)- The RTC reference crystal X3 needs tuning by C45 we do not know how critical this will be in production. RP2/8 and TR13 help minimise the power consumption. The open-drain I2C bus is pulled up by RP2/4,5. Note : the pull-ups are a diode drop above Vdd. The estimated power consumption is 50uA giving a five year battery life.

9.8 ECOnet

The clock detection circuit uses half a 74LS123, IC20. An incoming clock pulse triggers the monostable which has a time constant of approximately 20µs (2n2 and 39k C21,R59) thus generating a "Data Carrier Detect". If a subsequent pulse is not detected within 20µs the "Data Carrier Detect" signal is removed-

The chatter disconnect circuit uses half an 74LS123, IC20. This ensures that the transmitter does not hold the line for an unreasonable time thus jamming the network. This can only happen in error if the computer malfunctions. When a transmission is started "Request to Send" is asserted and the monostable triggered thus enabling the line driver, IC5. When the transmission finishes RTS is deasserted and the driver disabled. However should the monostable timeout before this the driver is again disabled. The time constant of the monostable is approximately 4.5seconds (100uP and 100k C22,R60). This value is calculated as follows.

The use of a 74LS123 NOT a 74HC123 is important as the trigger to output delay it much larger with the HC device.

slowest network 50E3 bits per second

largest packet	=	20E3 bytes
	=	160E3 bits
	=	200E3 bits after protocol overheads
time to transmit	=	200E3 / 50E3 seconds
	=	4 seconds

The Collision Detect circuit consists of two comparators, one for each of the DATA+ and DATA- anti-phase signals from the network. Comparisons (against the average of the two signals, plus a small offset) are only made against the active high period of each signal. In this way, even if the two signals have a high common mode offset both comparators will be switched off and CTS will be be de-asserted. As the data lines simultaneously go through high-low or low-high transitions, the comparators will indicate a transitory fault. An RC filter R71,C24 is used to remove these glitches. Its time constant is long enough to prevent false indication, but not long enough to completely mask the data bit following a transition.

9.9 Floppy Discs

The floppy disc interface will support up to four drives. The interface is useable with TTL and CMOS drives which may be 8", 5 1/4" or 3 1/2". The behaviour of drives has changed over time and a number of links arc provided to try and cope with this. The test point TP1 makes the controller *Head Load* signal available and the link LK7 allows the *READY* input to be disabled. The resistor-pack RP3 may need changing to match drive requirements. IC33 inverts the control lines as needed full buffering of this interface is not provided as it only drives internal discs on a short ribbon cable.

9.9.1 Floppy Disc controller

Either the FDC9793 or FDC1793, IC34, may be fitted. If the FDC1793 is used then LK12 must be made and C49 fitted. The data seperator IC32 is an external FDC9216B. This is digital and requires no adjustment, and allows software selection of the floppy disc data rates. IC4, IC15 and IC49 generate a software programable 1 or 2 MHz square wave for the floppy controller IC34. The floppy disc controller reset line is programmed independently of the system reset by *latchB* IC39.

9.9.2 Drive Powering

The floppy drive may be powered in one of two ways, either by a separate power connector or via the 34 way data cable SK7.

If conventional drives with seperate power connectors are used LK14 and LK15 should be changed.

9.9.3 Motor Control and the Little Red Light

The variations in specs are large. Beware.

9.9.4 Eject

The preferred eject is computer controlled so that the disc may not be removed until its state is guaranteed to be consistent.

9.10 Winchester Discs

The winchester disc interface will support up to two ST506 winchester drives. The control interface SK10 is daisy chained between drives. There is a separate data interface SK8 and SK9 for drives 0 and 1 respectively.

The control functions are all provided by a Hitachi HD63463 HDC. This contains all of the head control, data recovery, formatting, error correction/detection, MFM conversion, parallel/serial conversion and write precompensation facilities necessary to operate a Winchester hard disc. The data synchronisation and write precompensation timing is done by a National Semiconductor DP8465N-4 and associated chips.

9.10.1 Read data recovery

An analogue phase locked loop tuned to a nominal 5MHz data rate is fitted. The bandwidth allows for a +/- 1% speed variation of the media. The pll operates in two modes: A capture mode, where it is a frequency loop in which it attempts to lock onto the data's fundamental frequency. If it succeeds, it then waits until two bytes of zeros or ones have been recovered from the disc and issues a signal to permit the data to flow into the HD63463. This will prevent the HDC from being fed with a data stream that may include a write splice glitch causing it to abort the access. After a further two bytes, the HDC will indicate that it is following the bit stream and issue a SYNC signal to the pll, switching it from a frequency loop to a phase•only loop. The operating frequency is now constant until the end of the data block and only small phase changes are permissible in order to track the variable frequency bit stream.

Whilst locking, the pll's damping factor is about 1.15 and this gives it a typical locking distance of about two bytes. When locked, the damping factor falls to about 0.5 at 2-5MHz with a bandwidth of only some 30K rad/s.

When reading has stopped, the pll locks onto the 10MHz reference crystal so that a subsequent read operation finds the pll only 1% distant from its final locked on frequency.

The read data buffer IC49 is enabled by IC54/15, "lock detect", not "wgate" to prevent the controller attempting to detect sync bytes before the pll has locked. While the pll is locking R116 keeps read data low.

The read data path through the line receiver IC51 and the drive demultiplexer IC46 is inverting which is compensated for by connecting recieve + data to the inverting input.

9.10.2 Write data

Write precompensation is provided by a delay line of 10ns per tap. The appropriate tap is selected by the HDC Early/Late outputs. Nominal timing is obtained when neither of these are asserted. Write precompensation may be disabled by appropriate programming of the HDC. The write pre comp circuit may be bypassed by changing link LK16. MFM conversion is done by the HDC.

During writing, the pll locks onto the 10MHz reference crystal but the write data frequency is obviously determined by the HDC's connection to this same reference and not by the pll's connection to it.

The demultiplexing of EARLY/RGATE was found to be unnecessary and has been removed.

9.10.3 Large Drives

To allow drives with more than 8 heads to be used, the *reduced write current* pin of the ST506 interface may be reassigned as HS3 . This is then controlled by *latchB*.

9.10.4 Drive Power

Power is available on SK12 and SK13. The current power supply, the Master 128 PSU, is capable of running ONE low power 3 1/2" winchester. Because of the vicious demands of the drive the ports should be filtered to prevent noise injection to the main board.

9.11 Discs and RFI

The winchester drive generates a large amount of RFI with can interfere with the floppy disc drive. Care must be taken to provide adequate shielding.

9.12 Keyboard Interface

The IOC pins are protected by the inverting buffers in IC31 R95 erasure that the line idles LOW so that start bits are not detected if the keyboard is disconnected. R96 protects IC31 and R97 and C48 limit the slew rate and RFI. The 12volt output is not decoupled and should be. R98 ensures the machine is not reset when the keyboard is disconnected. R99 protects IC48 and C31 ensures that charge sharing does not cause the machine to be reset when a keyboard is connected. It has been suggested that C31 might be moved to the other side of R99 to protect an external switch.

9.13 POR and RESET

The internal reset signal RST may be driven either by a external source via the keyboard interface, pin 2 active LOW, or by the IOC. All sources are therefore open-drain and pulled high by RP2/8. R94 and C30 determin the length of the power-on reset pulse, this is order 1 second. This needs to be long enougth to pass the power surge of the winchester. D12 trys to discharge C30 if the power fails for a short time to ensure a full width reset pulse.

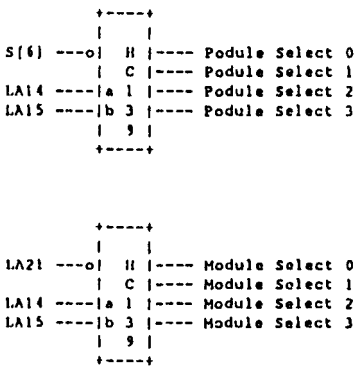
9.14 Expansion Podules and Backplane

All expansion for the A500 is by way of PODULES-.Every podule occupies at least one physical slot. All PODULES must obey the minimum attachment rules to allow correct mapping between PODULES, PHYSICAL SLOTS, and DEVICE DRIVERS. There are currently three classes of PODULES Simple Podules, MEMC podules and Co-processors. The backplane decodes the podule space into four podules and four MEMC: podules, using address lines LA[14:15]. Podules should be designed to be address independent and have a unique ID which allows the podule manager to bind drivers to physical addresses. However some early podule drivers are address specific and these podules must be located in the correct physical slot. R112 ensures that the podule id of a non-existent podule is read HIGH that not present.

9.14.1 Podule and Physical slots

There are four internal podule slots in the A500. A standard podule occupies a single podule slot. An extended podule occupies two podule slots horizontally. A podule is a single or double width, standard depth eurocard with a 96 way DIN connector. The main computer PCB has a single 96 way DIN connector into which a four way backplane is attatched. This backplane decodes the individual physical slots so that each slot occupies a different address space while keeping the physical characteristics of all four slots the same. This allows a podule to be inserted into any podule slot without changing links.

9.14.2 Ilackplane



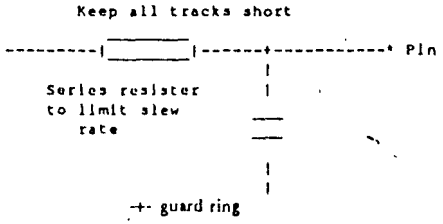
Note : delay on MS must meet IOAK setup and single N-cycle IOGT.

9.15 Fan

Yes, we have one, and it is powered from SK12 or SK13.

9.16 RFI

The main PCB has a guard ring which is an isolated track on the inner ground plane made available at TP2-TP5 and FT5. All connector shells and RFI components should be connected to this ring which is start wired to the PSU. The idea is that this ring will carry less noise than the ground plane despite its higher inductance. In practise the A500 has no RFI components but allows experimentation.



10. Programming Details

10.1 IOC Keyboard Asynchronous Receiver Transmitter (KART)

The KART provides an asynchronous serial link, to the keyboard- It is of fixed format with 8 bits to a character which is framed with one start bit and two stop bits. The least significant bit KD[0] is transmitted/received first. The KART divides into two halves, the receiver and the transmitter.

The ARM accesses the receiver via the *Serial Rx Data register.* A clock of 16 times the data rate is used by the KART to clock in the serial data from the KIN pin. When a data byte has been received, the SRx bit is asserted in the *IRQ Status B Register* to indicate that the byte is available for reading. False start bits of less than a half bit duration are ignored.

The ARM accesses the transmitter via the *Serial Tx Data register.* The byte written to the *Serial Tx Data register* is transmitted serially from the KOUT pin, and the *STx* bit is asserted in the *IRQ Status B register* to indicate that the transmission is finished and the *Serial Tx Data register* may be reloaded.

The receive and transmit speeds are the same and are programmed using counter 3.

10.1.1 Serial Tx Data register

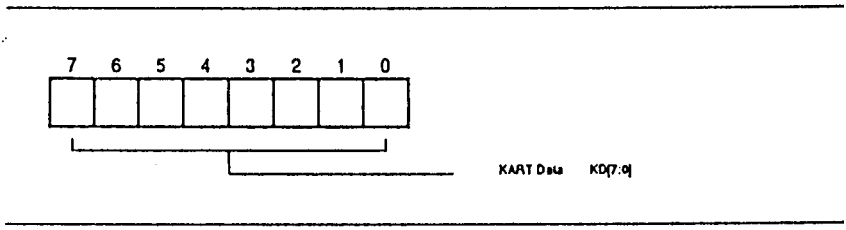


Figure 6: Serial Tx Data register 04H write

Writing to this register loads the serial output shift register, clean any outstanding TRx: interrupt and starts the transmission. An interrupt is raised when the register is ready to be reloaded.

10.1.2 Serial Rx Data register

Reading from this register clears any outstanding SRx interrupt and returns the currently received byte. Data is only valid while the SRx bit is set in the *IRQ status B register.*

10.1.3 Initialisation

After Power-On, the KART is in an undefined state. The KART is initialised by programming the serial line speed using counter 3 and performing a read from the *Serial Rx Data register,* discarding the data byte. This will clear any outstanding receive interrupt and enable the KART for the next reception. Finally the *Tx Data register* should be written to. This will abort any transmission in progress, cause a new one to be started, and clear any STx interrupt.

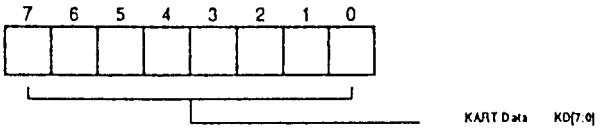


Figure 7: Serial Rx Data register 04H read

10.1.4 Receive Interrupt

The SRx interrupt is set halfway though the reception of the last data bit. Care should be taken to ensure that the last bit has been received before the *Serial Rx data register* is read, to prevent this bit being interpreted as the start bit of the next packet.

10.2 External Latch A

The Exsernal Latch A is a write only latch used to control parts of the floppy disc sub-system.

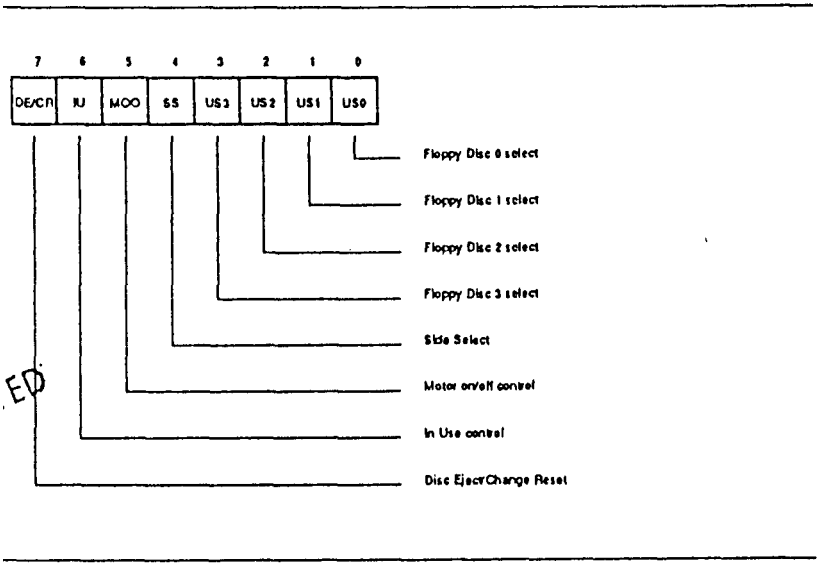


Figure 8: External Latch A 3360000H

10.2.1 Bit [0:3] US[0:3]

These bits select the floppy disc unit 0 through 3 when written LOW. Only one bit should be LOW at any one time.

10.2.2 Bit 4 Side Select

This controls the side select line of the floppy disc interface.

0 = Side 1 upper
1 = Side 0 lower

10.2.3 Bit 5 Floppy Motor ON/OFF Control

This bit controls the floppy disc motor line. Its exact use depends on the type of drive.

10.2.4 Bit 6 In Use

This bit controls the INUSE line of the floppy disc. 1ts exact use depends on the type of drive.

10.2.5 Bit 7 Disc Eject

This controls the DISC EJECT or DISC CHANGED RESET line of the floppy disc drive.

10.3 External Latch B

The *External Latch B* is a write only register shared between several users who must maintain a consistent RAM copy. Updates must be made with 1RQ disabled.

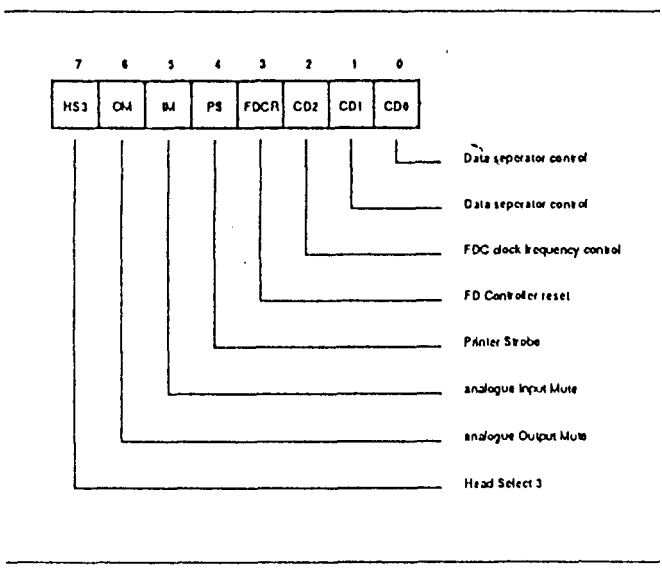


Figure 9: External Latch B 3350018H

10-3.1 Bit [0:2] CD[0:2]

These bits control the Floppy disc data rate and format. The following settings are meaningful.

CD[2:1:0]	Function
0 0 0	600 rpm DD/300 rpm QD
1 0 1	600 rpm SD/300 rpm DD
1 1 0	300 rmp SD

Name	density	f/s
SD	single	DFS
DD	double	ADFS/PCDOS
QD	quad	OAK

10.3.2Bit 3 FDCR

This controls the Floppy Disc Controler Reset Line. When programmed LOW the controller is RESET.

10.3.3 Bit 4 Printer Strobe

This is used to indicate valid data on the printer outputs. It should be set HIGH when valid data has been written to the printer port and LOW after a typically 5µ seconds.

10.3.4 Bit 5 IMute

When set HIGH the analogue Input AIN is muted. When LOW AIN is mixed with the VIDC sound output and fed to the speaker.

10.3.5 Bit 6 OMute

When set HIGH the analoge output AOUT is muted.

10.3.6 Bit 7 HS3

This bit controls the HS3 line of the winchester disc interface. It allows extension of the ST506 interface to support upto 16 heads. It may be disabled by LK16 and LK17 to implement the standard ST506 "*Reduced Write Current*" function.

10.4 Interrupts

The IO system generates two independent interrupt requests, IRQ and FIQ- Interrupt requests can be caused by events internal to IOC or by external events on the interrupt or control port input pins-

The interrupts are controlled by four types of register, status, mask, request and clear. The status registers reflect the current state of the various interrupt sources. The mask registers determine which sources may generate an interrupt. The request registers are the logical AND of the status and mask registers and indicate which sources are generating interrupt requests to the processor. The clear register allows clearing of interrupt requests where appropriate. The mask registers are undefined after power up.

The IRQ events are split into two sets of registers A and B . There is no priority encoding of the sources.

Internal Interrupt Events

- Timer interrupts TM[0:1].
- Power-on reset POR.
- Keyboard Rx data available SRx.
- Keyboard Tx data register empty STx.
- Force interrupts "I".

External Interrupt Events

- IRQ active low inputs IL[0:7] wired as PFIQ,SIRQ,SLCI,WIRQ,WDRQ,PIRQ,PBSY and RII.
- IRQ falling-edge input IF wired as PACK.
- IRQ rising-edge input IR wired as VFLY.
- FlQ active high input FH[0:1] wired as FFIQ and FFDQ.
- FIQ active low input FL wired as EFIQ.
- Control port inputs C[3:5]

Level Interrupts

The majority of external and a few of the internal interrupt sources are level sensitive. When one of these sources has caused an interrupt it is cleared by removing the source.

Latched interrupts

The IF. IR. POR and TM[0:1] sources are latched. That is, once one of these sources has caused in interrupt, it must be cleared by an explicit write of "1" to the appropriate bit in the *IRQ Clear aAregister.* One or many may be cleared in a single operation.

Synchronisation

All the interrupt sources are synchronised by the REF8M clock input. It can take up to three clock phases before a source is recognised as requesting an interrupt, and the same delay occurs between a level sensitive request going inactive at an input pin and the removal of the corresponding bit from the status register and the processor interrupt line.

10.5 IRQ Status A

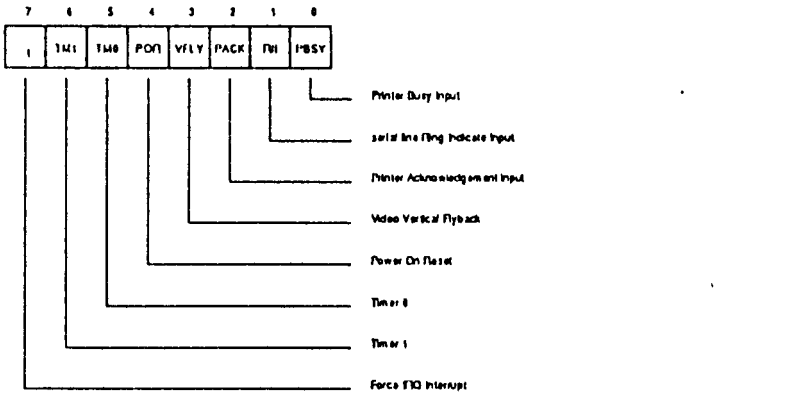


Figure 10: IRQ Status A 3200010H read

10.5.1 Bit 0 PBSY

This bit indicates that the printer is busy.

10.5.2 Bit 1 RII

This bit indicates that a Ringing Indication has been detected by the serial line interface.

10.5.3 Bit 2 Printer Acknowledge

This bit indicates that a printer acknowledge pulse has been received.

10.5.4 Bit 3 Vertical flyback

This bit indicates that a vertical flyback has commenced.

10.5.5 Bit 4 Power-on Reset

This bit indicates that a power-on reset has occurred.

10.5.6 Bit [5:6] Timer 0 and Timer 1 events

These bits indicate that timer events have occurred.

Note : latched interrupt.

10.5.7 Bit 7 Force

This hit is used to force an IRQ request. It is usually owned by the FIQ owner and is used to downgrade FIQ requests into IRQs.

10.6 IRQ Status B

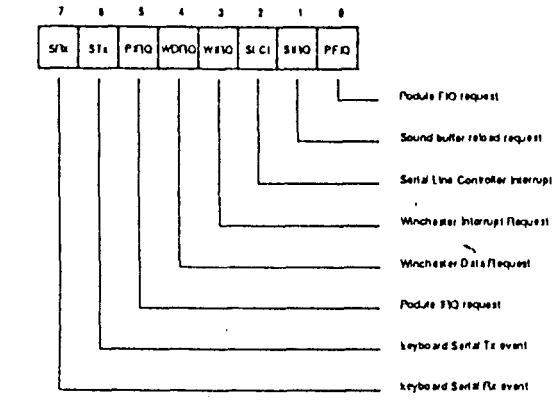


Figure I1: IRQ Status 3200020H read

10.6.1 Bit 0 Podule FIQ request

This bit indicates that a podule FIQ request has been received. It should usually be masked OFF.

10.6.2 Bit 1 Sound buffer swap

This bit indicated that the MEMC sound buffer pointer has been reloaded.

10.6.3 Bit 2 Serial line controller

This bit indicates that a 65C51 serial line controller interrupt has occured.

10.6.4 Bit 3 Winchester Interrupt

This bit indicates that a Winchester interrupt has occured.

10.6.5 Bit 4 Winchester data request

This bit indicates that a Winchester data request has occurcd.

10.6.6 Bit 5 Podule Interrupt request

This bit indicates that a Podule IRQ request has occured.

10.6.7 Bit 6 Keyboard transmission event

This bit indicates that the keyboard transmit register is empty and may be reloaded.

10.6.8 Bit 7 Keyboard reception event

This bit indicates that the keyboard reception register is full and may be read..

10.7 Interrupt Status FIQ

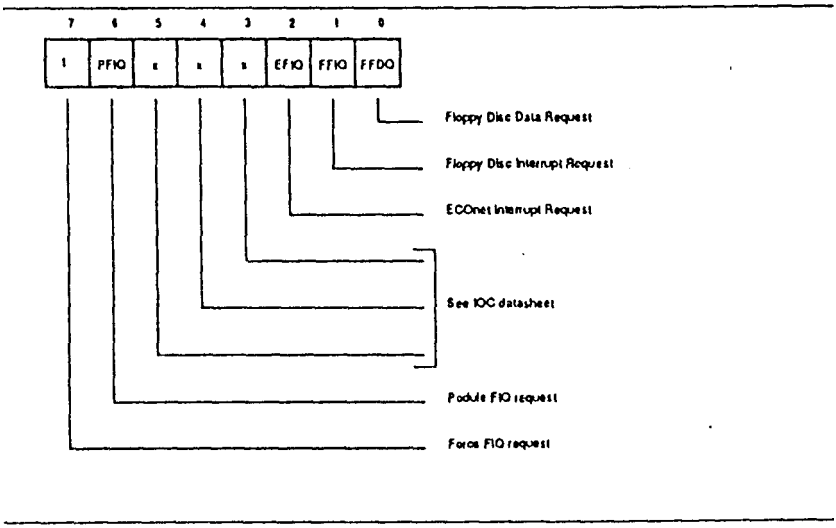


Figure 12: Interrupt Status FIQ 3200030H read

10.7.1 Bit 0 floppy disc data request

This bit indicates that a Floppy Disc Data Request has occured.

10.7.2 Bit 1 Floppy disc Interrupt request

This bit indicates that a Floppy Disc Interrupt Request has occured.

10.7.3 Bit 2 ECOnet Interrupt request

This bit indicates that a ECOnet Interrupt Request has occured.

10.7.4 Bit [3:5] Undefined

See IOC data sheet for details.

10.7.5 Bit 6 Podule FlQ request

This bit indicates that a podule FIQ Request has occured.

10.7.6 Bit 7 Force

This bit allows an FIQ interrupt request to be generated.

10.8 IRQ Clear register

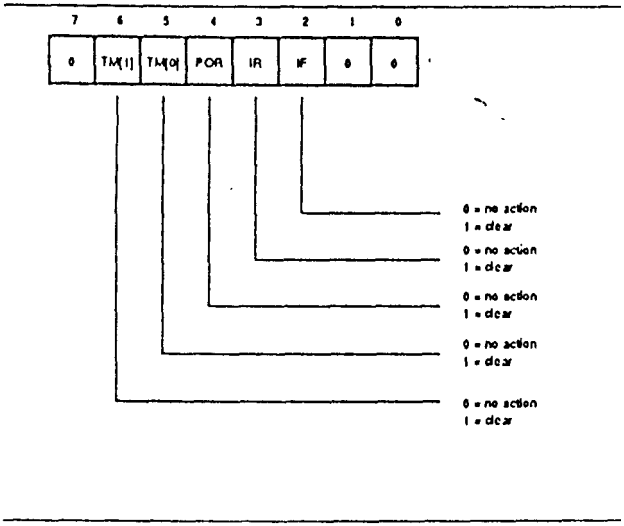


Figure 13: IRQ Clear register 14H write

10.9 Interrupt Request registers 3200014H 3200024H 3200034H read

These registers show which interrupt sources are currently enabled and active. They give the logical AND of the corresponding *status and mask* registers.

(i) IRQ request A address 32000141H
(ii) IRQ request B address 32000241H
(iii) FIQ request address 32000341H

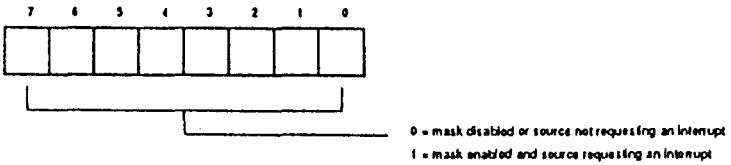


Figure 14: Request registers

10.10 Interrupt Mask registers 3200018H 3200028H 3200038H read/write

The *mask registers* are readable to simplify the sharing of these registers between a number of interrupt handlers.

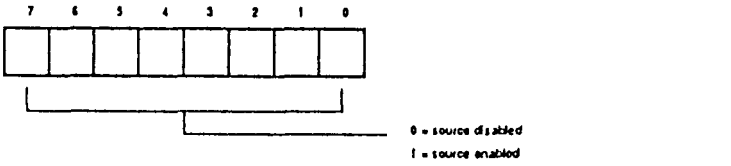


Figure 15: Mask registers

(i) IRQ mask A address 3200018H
(ii) IRQ mask B address 3200028H
(iii) FIQ mask address 3200038H

10.11 Control Port

The *control register* allows the external control pins C[0:5] to be read and written and the status of the PACK and VFLY inputs to be inspected. The C[0:5] bits manipulate the C[0:5] IO Port. When read, they reflect the current state of these pins. When written LOW the output pin is driven LOW. These outputs are open-drain, and if programmed HIGH the pin is undriven and may be treated as an input.

On reset all bits in the control register are set to "1".

10.11.1 C[0:1) The I2C

The C[0:1] pins are used to implement the bi-directional serial I2C bus to which the Real Time Clock and battery RAM are connected. For further details see PCF8570 and PCF8573 data sheets.

10.11.2 Control port read

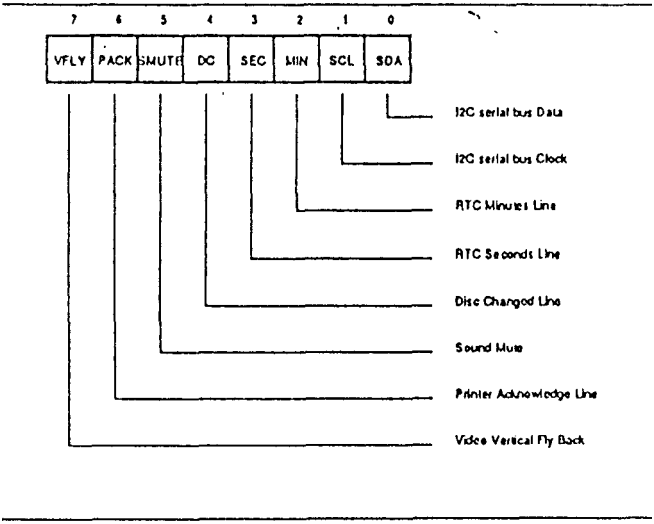


Figure 16: Control port 3200000H read

10.11.3 Control port write

C[6:7] control internal test modes and if programmed to 0 will cause the counters and KART to malfunction.

In the A500 C[2:4] are wired as inputs and if these bits are programmed to 0 they will become outputs causing excessive current to be draw by the chip.

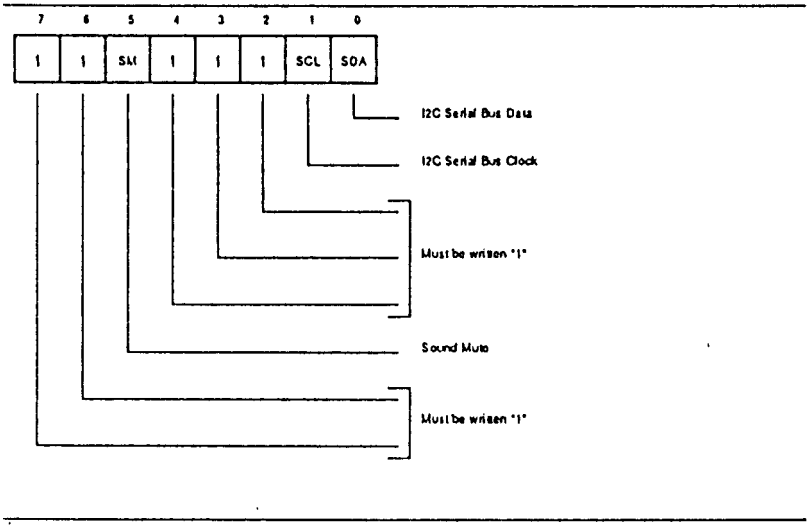


Figure 17: Control port 3200000H write

10.12 Counters

Four identical 16 bit counters are provided. Two are used as timers, the third for the keyboard BAUD rate and the fourth as a general purpose output. They all have fully programmable start/reload values.

Each counter consists of a 16 bit down counter, a 16 bit input latch (*latch low* and *latch high*) and a 16 bit output latch (*count low* and *count high*) which contains the value of the counter when the *latch command* is given. The counter decrements continuously, clocked at 2 MHz. When it decrements to zero, it is reloaded from the *input latch* and recommences decrementing. The reload is used to trigger different events depending on the use of the counter. If a counter is loaded with zero it continuously reloads and does not count. If the *GO register* is written at the same time as the counter reloads an extra 2 MHz clock tick is taken o reload. After power-on the state of the counters is unknown.

latch = latch low + 256 * latch high

10.12.1 Register actions

Latch low	Writing to this updates the low order byte of the input latch
Latch high	Writing to this updates the high order byte of the input latch
GO command	Writing to this causes the counter to be reloaded immediately with the latch value.
Count low	This causes the low order byte of the output latch to be read.
Count high	This causes the high order byte of the output latch to be read.
Latch command	This causes the current value of the counter to be placed in the output latch.

10.12.2 Counter schematic

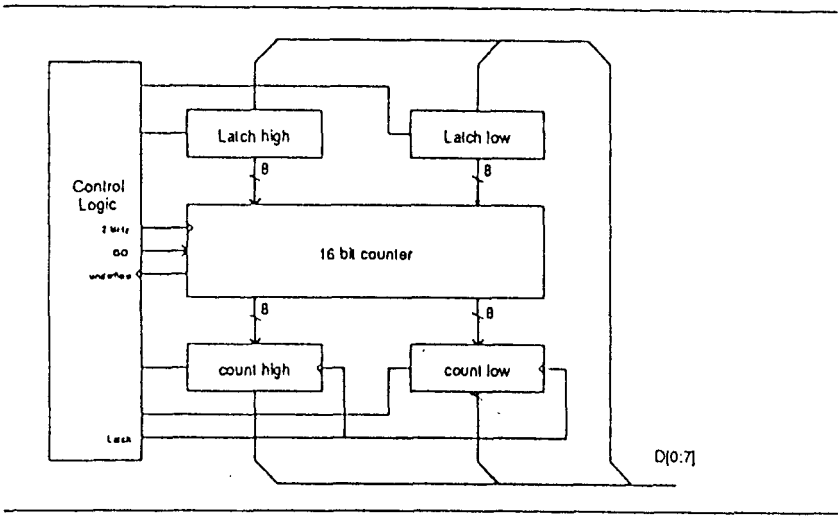


Figure 13: Counter schematic

10.12.3 Counter Registers

	Address for counter				read or
	0	1	2	3	write
Latch low	40H	50H	60H	70H	write
Latch high	44H	54H	64H	74H	write
GO command	48H	58H	68H	78H	write
Count low	40H	50H	60H	70H	read
Count high	44H	54H	64H	74H	read
Latch command	4CH	50H	6CH	7CH	write

10.12.4 Counters 0 and 1

Two general purpose timers are provided. The reload event sets a timer interrupt, TM[0:1] in the *IRQ status A register*. The interrupt is cleared via the *IRQ Clear A register*. In order to generate an interrupt after time $T_{interval}$ the 16 bit value, (*latch*), to be used is calculated from the following equation.

$$T_{interval} = latch/2\ \mu seconds$$

10.12.5 Counter 2 (BAUD)

The counter 2 output is used to drive the BAUD pin. The reload event toggles the BAUD clock line. In order to generate a clock of frequency f_{BAUD}, the 16 bit value, (*latch*), to be used is calculated from the following equation.

$$f_{BAUD} = 1/(latch+1)\ MHz$$

The maximum BAUD rate of 500kHz is obtained by programming *latch* = 1.

10.12.6 Counter 3 (KART)

The counter 3 output controls the speed of the keyboard serial link. In order to generate a baud rate k_{BAUD}. the 16 bit value, (*latch*), to be used is calculated from the following equation.

$$k_{BAUD} = 1/((latch+1)*16) \text{ MHz}$$

The maximum baud rate of 31250Hz is obtained by programming *latch=1*.

11. Reset and Power-on

The A500 may be reset in two ways: by driving the bidirectional RST line LOW, or by driving the POR line LOW. The RST line in connected to the reset switch on the back right of the keyboard. Pressing this will reset both the keyboard and the A500. The POR pin is connected to an RC network to ensure that when power is first applied to the A500, a system reset signal is generated on RST.

POR causes an internal latched interrupt to be set to allow system software to differentiate between "power-on" and "soft" resets, and ensures that peripheral chips have had a stable clock for a suitable length of time before being released from reset. The keyboard may be unplugged and replugged without reseting the A500 as it contains its own power-on reset circuit. The control register is initialised on reset causing the C[0:5] pins to be set to a known state, before the processor commences execution.

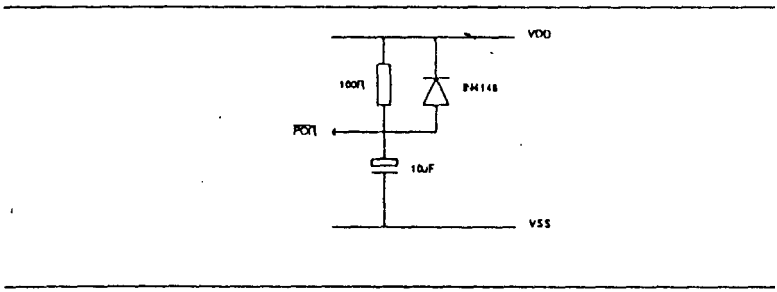


Figure 19: A500 power-on reset circuit

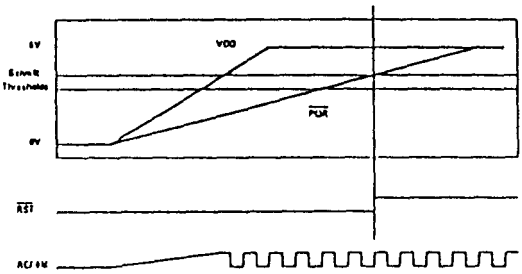
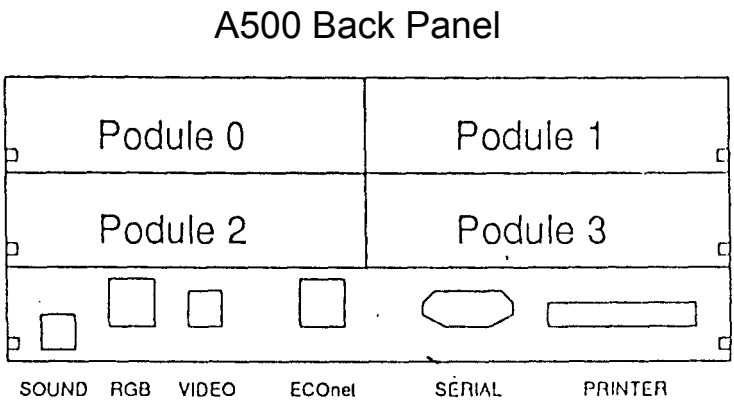


Figure 20: Power-on timing

12. Mechanical



12.1 Construction

12.2 Installing Podules

12.3 The Disc Tray

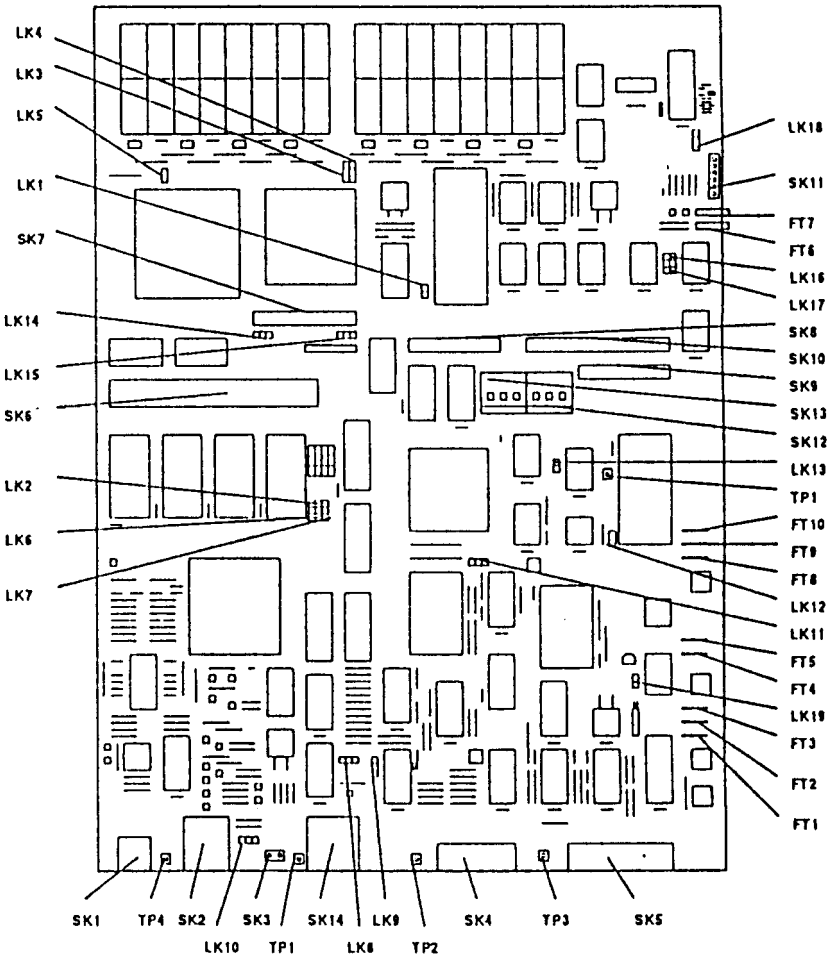
12.4 Removing the Main PCB

12.5 Changing the flatteries

12.6 Changing the ROM's

12.7 Air flow

13. Main PCB Connectors, Links and Test Points



13.1 TP1 HLD Head Load

This test point makes the HDC head load output available.

13.2 TP2-TP5 Guard rail

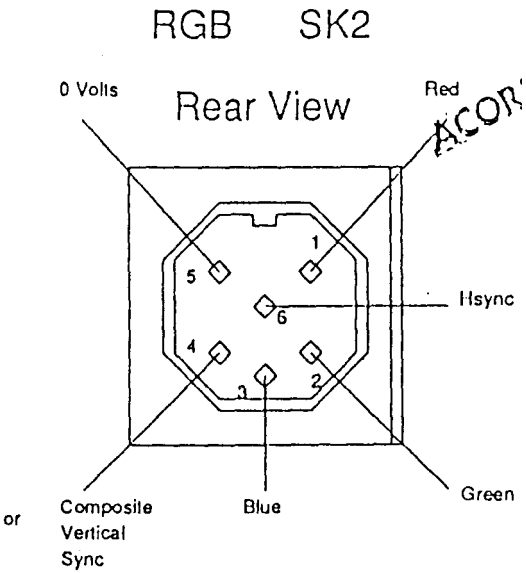
These test points make the GUARD rail available.

13.3 SK1 Audio Output

This connector provides STEREO audio output.

13.4 SK2 RGB Video output

This connector provides the RGB and sync outputs.



13.5 SK3 Monochrome video output

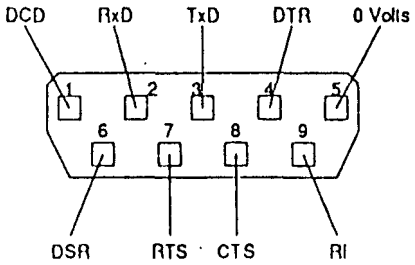
This connecter provides Monochrome Video.

13.6 SK4 RS423 Serial line

This plug ptovides an "AT" serial line interface to the RS423 standard.

Serial SK4

Rear View



13.7 SK5 Parallel printer connector

This connector provides a parallel printer interface.

Pin	Function	Pin	Function
1	STB	14	0V
2	0V	15	D6
3	D0	16	0V
4	0V	17	D7
5	D1	18	0V
6	0V	19	ACK
7	D2	20	0V
8	0V	21	BSY
9	D3	22	0V
10	0V	23	n/c
11	D4	24	0V
12	0V	25	n/c
13	D5	26	n/c

13.8 SK6 Podule backplane expansion

This connect may be used to attatch one PODULE or the expansion backplane.

Pin	a	b	c (Backplane)	c (Podule)
32	V5	D[31]	V12	V12
31	BD[0]	.	CLKSYS	CLKSYS
30	BD[1]	.	V5	V5
29	BD[2]	.	REF8M	REF8M
28	BD[3]	.	CLK8	CLK8
27	BD[4]	.	CLK2	CLK2
26	BD[5]	.		
25	BD[6]	.	BL	BL
24	BD[7]	.	NIOAK	NIOAK
23	BD[8]	.	NIOGT	NIOGT
22	BD[9]	.	S[6]	PS
21	BD[10]	.	S[7]	S[7]
20	BD[11]	.	C0	C0
19	BD[12]	.	C1	C1
18	BD[13]	.	EFIQ	EFIQ
17	BD[14]	.	NPFIQ	NPFIQ
16	BD[15]	.	NPIRQ	NPIRQ
15	LA[2]	.	NPRE	NPRE
14	LA[3]	.	NPWE	NPWE
13	LA[4]	.	LRNW	LRNW
12	LA[5]	.	NRST	NRST
11	LA[6]	.	PHI1B	PHI1B
10	LA[7]	.	OPC	OPC
9	LA[8]	.	CPI	CPI
8	LA[9]	.	CPB	CPB
7	LA[10]	.	CPA	CPA
6	LA[11]	.	LA[21]	MS
5	LA[12]	.	AGND	AGND
4	LA[13]	.	AOUT	AOUT
3	LA[14]	.	AIN	AIN
2	LA[15]	.	V-5	V-5
1	V0	D[00]	V0	V0

13.9 SK7 Floppy disc drive conRector

This socket is used to connect o the FD. Power may be supplied via this cable or seperately. See LK14 and LK15.

Pin	Function	Pin	Function
1	disc eject	18	DIR
2	n/c	19	0V
3	5V or 0V	20	STEP
4	in use	21	0V
5	5V or 0V	22	Write Data
6	SEL 3	23	0V
7	5V or 0V	24	Write Gate
8	index	25	0V
9	5V or 0V	26	Track 00
10	SEL 0	27	0V
11	5V or 0V	28	Write Prot
12	SEL 1	29	12V or 0V
13	0V	30	Read Data
14	SEL 2	31	12V or 0V
15	0V	32	Side Sel
16	Motor On	33	12V or 0V
17	0V	34	Ready

13.10 SK8 and SK9 Winchester data connector

These two connector are used to attatch the winchester disc drives.

SK8 for DRIVE 0
SK9 for DRIVE 1

Pin	Function	
13	Write Data +	
14	Write Data -	
17	Read Data +	
18	Read Data -	
2,4,6,8,11,12,15,16,19,20		0 Volts
1,3,5,7,9,10		n/c

13.11 SK10 Winchester control connector

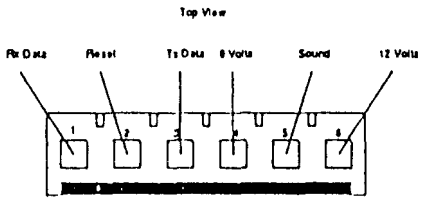
This connecor is used for the daisy chain winchester control cable.

Pin	Function	Pin	Function
1	0V	18	HSEL1
2	RWC or HS3	19	0V
3	0V	20	INDEX
4	HSEL2	21	0V
5	0V	22	DRDY
6	NC	23	0V
7	0V	24	STEP
8	SC	25	0V
9	0V	26	DSEL0
10	TRK00	27	0V
11	0V	28	DSEL1
12	WFLT	29	0V
13	0V	30	n/c
14	HSEL0	31	0V
15	0V	32	n/c
16	n/c	33	0V
17	0V	34	DIRIN

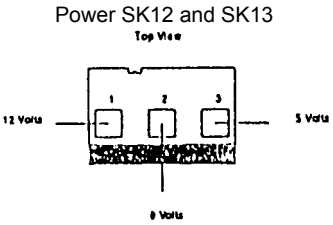
13.12 SK11 Keyboard connector

This socket is used to connect the keyboard

Keyboard SK11

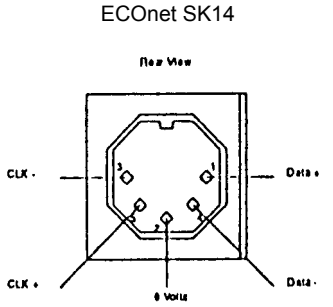


13.13 SK12 and SK13 Power connectors



13.14 SK14 ECOnet connector

This socket provides the standard ECOnet interface



13.15 LK1 20/24MHz Clock option

This link is OPEN for 20MHz ARM's with X4 fitted. This link is MADE for 24MHz ARM's with X4 not fitted.

13.16 LK2 ROM expansion

This link is normally made and allows for ROM expansion.

13.17 LK3 and LK4 1M/256k RAM option

These links select 256k or 1M bit DRAMS

13.18 LK5 3/2µ ARM option

This link is normally MADE for 3µ ARM and broken for 2µ ARM.

13.19 LK6 and LK7 ROM size option

These links select the size of the system ROMS to be 256K or 128k or 512k.

Link 6	7	ROM size
A	A	128k
A	B	do not use
B	A	256k
B	B	512k

13.20 LK8 Monochrome video option

This link selects 1 bit 96MHz or 2 bit 48MHz video.

13.21 LK9 VIDC speed select

Hight resolution video speed select on test.

A	VIDC 18 to 41 nS
B	VIDC <28 or >38 nS

13.22 LK10 Monochrome video option

This link selects composite monochrome video of high resolution video without sync as selected by LK8.

13.23 LK11 Unused IOC input

This link is connection to the IOC i/o o/d C[4] pin. It may be used as an output or an input.

13.24 LK12 FDC power option

This link selects 12 Volts on Pin 40 of the FDC. Its is normally OPEN to allow the use of WD9793. It should be made to use the WD1793.

13.25 LK13 FDC ready option

This link is normally OPEN to allow the use of FD drives that generate a READY signal. For drives that do not generate READY this link should be made.

I3.26 LK14 and LK15 Floppy Drive power option

These links are normally MADE to provide power for the floppy disc via the ribbon cable. They should be both cut and linked to "0" for external powering.

13.27 LK16 Winchester write-precomp option

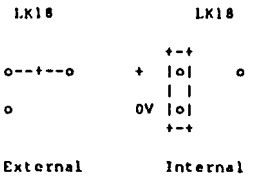
This link allows write data precomp to be disabled should we purchase drives that do not require it. This link is normally MADE to enable write precomp.

13.28 LK16 and LK17 Winchester RWC or HS3 option

These two links are used to select "Reduced Wtite Current" or "Head Select 3" on pin 2 of the Winchester control cable. See Extended Register bit 15.

13.29 LK18 Speaker

This link is normally made and routes the speaker output via the keyboard connector SK11. The MOLEX header allows an internal speaker to be connected.



13.30 LK19 RTC frequency TEST

This link has 0 volts and the Real Time Clock buffered frequency output to allow fine adjustment of the crystal oscillator.

13.31 IC10 Video header

Do we want to say anything here?????

13.32 Power Connections

FT1	+5 Volts
FT2	0 Volts
FT3	-5 Volts
FT4	+5 Volts
FT5	GUARD
FT6	BATTERY +3 Volts
FT7	BATTERY 0 Volts
FT8	+12 Volts
FT9	+5 Volts
FT10	0 Volts

14. A500 Parts List

14.1 Main PCB

14.1.1 Integrated Circuits

		TYPE	NO./MC
IC1		TL072	1
IC2		4053	1
IC3		74F04	1
IC4		74F74	1
IC5,IC7		AM26LS30	2
IC6,IC51		AM26LS32	2
IC8		74LS574	1
IC9		TL074	1
IC10	NOT FITTED	HEADER	1
IC11		74F194	1
IC12		10174	1
IC13,IC14		LM319	2
IC15,IC43,IC52		74HC04	3
IC16		VIDC	1
IC17,IC18		74HCT573	2
IC19		68B54	1
IC20		74HC123	1
IC21		65C51	1
IC22		PCF8573	1
IC23		PCF8570	1
IC24-IC27		27128	4
IC28,IC29,IC35-IC37		74HC573	5
IC30		IOC	1
IC31,IC48		74HCT14	2
IC32		FDC9216B	1
IC33,IC47		7406	2
IC34		FDC9793	1
IC38,IC39		74HC574	2
IC40		74HC139	1
IC41		ARM	1
IC42		MEMC	1
IC44		HD63463	1
IC45		AM26LS31	1
IC46		74HC51	1
IC49		74HCT125	1
IC50		7438	1
IC53		74HCT153	1
IC54		DP8465	1
(IO55-IO86		411000	32

14.1.2 Capacitors

	VALUE	TYPE	NO/MC
C51,C52	22pF		2
C25,C41	33pF		2
C19,C20,C26-C28	47pF		5
C4,C5,C10,C11	330pF		4
C21,C34	1n		2
C2,C3,C8,C9	3n3		4
C24,C48	10nF		2
"A"x80,C6,C7,C12, C13,C39,C40,C46,C47	33nF	Decouplers	88
C38	100nF	Poly	1
C1	470nF	Poly	1
C37	1uF	Poly	1
"B"x8	4u7 10V	Decouplers	8
C14-C18,C23,C29,C30, C31	10uF 10V	Tant	9
C50	10uF 16V	Tant	1
C22,C42,C43,C44	100uF 16V	Elec	4
C35	68nF 10%		1
C36	2x 47pF		2
C32,C33	NOT FITTED		0
C45	12pF		1
C49	NOT FITTED		0

Note 1 : fit C51 between R6 and R7
2 : fit C52 between R17 and R18
3 : cut LK15 and fit 100uF 16v elec

14.1.3 Resistors

	VALUE	NO./MC
R58,R105	47R	2
R28,R29,R56,R57,R200-R231	68R	36
R96,R99,R110,R111	100R	4
R48,R49,R50,R107	150R	4
R30,R31,R32,R35,R38,R55,R97,R109	220R	8
R47,R51,R52	330R	3
R33,R34,R36,R37,R39,R40	470R	6
R103,R104	820R	2
R14,R15,R25,R26,R43,R61,R63, R71,R81,R82,R114	1K	11
R44	1K5	1
R54	2K7	1
R1,R2,R90,R91,R92,R93,R102, R113,R115	4K7	9
R41,R42,R83,R84,R85,R87,R88, R95,R98,R112,R116	10K	11
R3	15K	1
R7,R8,R9,R18,R19,R20	22K	6
R27	33K	1
R6,R17	39K	2
R5,R16,R59,R60,R94,R108	100K	6
R10,R11,R12,R13,R21,R22,R23,R24	150K	8
R4	330K	1

R62,R64,R74	1M5		3
R66,R106	1K	1%	2
R53,R65	1K5	2%	2
R67,R68,R69,R70	10K	2%	4
R72,R73,R75,R76	56K	2%	4
R77,R78,R79,R80	100K	2%	4
R100,R101	NOT FITTED		0
R45,R46,R86,R89,R117-R199	DO NOT EXIST		

RP1,RP2,RP5	4K7		3
RP3	1K		1
RP4	220/330R	AB 850 85	1

Note 1 : RP1-5 are 8 pin SIL's
2 : R44 is fitted between IC28/11 and IC28/20

14.1.4 Diodes

	TYPE	NO./MC
D1-D3	BZX79C2V7	3
D4-D12	1N4148	9

14.1.5 Transistors

	TYPE	NO./MC
TR1-TR8,TR11,TR13	2N3904	10
TR9,TR10,TR12	2N3906	3

14.1.6 Misc

	VALUE	TYPE	NO./MC
X1	48MHz	HC18/U	1
X2	1.8432MHz	HC18/U	1
X3	32768Hz	38	1
X4 NOT FITTED	20MHz		0
X5	10MHz	HC18/U	1
L1,L2	33uH		2
L3	0.33uH		1
DL1	PE21198-A		1
PCB	0000 025 B		1

Note 1 : Cut LK14 and fit 5uH inductor

14.1.7 Connectors

	TYPE	NO./MC
TP1	not fitted	0
TP2-TP5	not fitted	0
SK1	Mini-jack	1
SK2	6 Way DIN socket	1
SK3	BNC panel mounting 75R	1
SK4	9 Way D Male	1
SK5	26 Way IDC socket Rt/angle	1
SK6	96 Way abc DIN 41612 Socket	1
SK7,SK10	34 Way IDC boxed header	2
SK8,SK9	20 Way IDC boxed header	2
SK11	6 Way 6410 Series	1
SK12,SK13	3 Way 5414 Series	2
SK14	5 Way DIN socket 180'	1.

Note : SK4 NEEDS TO BE FIXED BY TWO M3x10 SCREWS AND NUTS.

FT1,FT2,FT3,FT4, FT5,FT8,FT9,FT10	Faston tab st	8
FT6,FT7	Faston tab rt/angle	2

14.1.8 IC Sockets

	NUMBER OF PINS	NO./MC
IC41	84 Jedec	1
IC16,IC42	68 Jedec	2
IC30	68 Jedec C	1
IC10	14 dil	1
IC5	16 dil	1
IC55-IC86	18 dil	32
IC19,IC21,IC24, IC25,IC26,IC27	28 dil	6
IC34	40 dil	1
IC44	48 dil	1
IC54	24 skinny-dip	1

14.1.9 Links

	NUMBER OF PINS	NO./MC
LK1,LK19	2	2
LK8,LK9,LK10	3	3
MOLEX SHUNTS	2 WAY	5

LK2,LK3,LK4,LK6,LK7, LK11,LK12,LK13,LK14, LK15,LK16,LK17,LK18 THESE LINKS ARE NOT FITTED

14.2 PSU

The A500 uses the Master 128 PSU. This is a compromise and is probable inadequate for a production machine. It was however readily available

14.3 Disc Sub-System

14.3.1 Floppy Disc

14.3.2 Winchester Disc

14.3.3 Batterys

14.4 Fan

15. Modifications

These modifications are necessary on Issue B boards

(1) Compensate the Op Amp for driving large capacitive loads. see "capacitors" notes 1 and 2.

(2) Smoothing +12 volts to the floppy disc drive. see " capacitors" note 3.

(3) Reduce BL pullup to 1K2
see "resistors" note 2.

(4) Put DHEi instead of CHSYS on the podule bus.
REMOVE IC43/6 and LINK IC43/9 to IC43/6.

(5) Reduce IOAK pullup to 1K5.
LINK RP5/6 to RP5/7 to RP5/8.

(6) Smooth +5 volts to the floppy disc drive. see "Misc" note L

(7) ECOnet collision detect modification.
Fit 33pF between IC14/7 and IC14/8. Link IC14/1/2/3/14/15. Link IC13/1/2/3/13/14.

(8) Split external latching into LatchA and LatchB.
Cut track IC38/11 to IC39/11. Link 1C30/57 to IC38/11.

16. Appendix A Keyboard Protocol

The ARM to keyboard connection is essentially a half duplex connection with hand shaking by the ARM, plus a small amount of command protocol by the ARM. Overrun in the keyboard is avoided partly by the half duplex nature of the connection and partly by a sufficiently low interrupt latency. Overrun in the ARM is avoided by acknowledging precisely when a byte is received, and at no other time.

When the keyboard has sent a byte, in normal operation, it will not send again until it has received an Ack from the ARM. The only exception to this is during the reset protocol used to synchronise the handshaking, where each side is expecting specific responses from the other, and will not respond further until it has those. Unexpected responses cause the reset sequence to be restarted.

Timeout by the ARM should take some appropriate action such as informing the user his keyboard isn't plugged in, or is naff. Timeout by the keyboard doesn't exist, as there is nothing it could usefully do.

In addition to this simple handshaking system, the keyboard will not send mouse data unless specifically allowed to, as indicated by Ack Mouse, which allows the transmission of one set of accumulated mouse coordinate changes, or the next move made by the mouse. While it is not allowed to send mouse changes the keyboard will buffer mouse changes, though if these become large they wili become meaningless.

A similar handshake exists on key changes, transmitted as key up and key down, and enabled by Ack Scan. At the end of a keyboard packet (two bytes) ARM should always Ack Scan, there is no protocol for re-enabling later. With the mouse the situation is different, the ARM may request mouse data some time later by means of request mouse position.

Keyboard to ARM

Type	d7	d6	d5	d4	d3	d2	d1	d0	Number of Bytes	
Reset	1	x	x	x	x	x	x	x	1	
Key up	0	0	1	1	x	x	x	x	2	(row then column)
Key down	0	0	1	0	x	x	x	x	2	(row then column)
Mouse change	0	1	x	x	x	x	x	x	2	(X, Y)
SPD data	0	0	0	0	x	x	x	x	1	
Keyboard id	0	0	0	1	x	x	x	x	2	(low nibble then high nibble)

ARM to Keyboard

LED on	0	0	0	0	x	x	x	x	1	(There is only one LED)
LED off	0	0	0	1	x	x	x	x	1	
Request	0	0	1	0	x	x	x	x	1	
Ack	0	0	1	1	x	x	x	x	1	
SPD data	0	1	0	0	x	x	x	x	1	(nibble to be converted)
Reset	1	x	x	x	x	x	x	x	1	

Reset types

Hard reset	1	1	1	1	1	1	1	1	1
Reset ack 1	1	1	1	1	1	1	1	0	1
Reset ack 2	1	1	1	1	1	1	0	1	1

Request types

KbId	0	0	1	0	0	0	0	0	1
SPDReset	0	0	1	0	0	0	0	1	1
Mouse position	0	0	1	0	0	0	1	0	1

Ack types

Byte	0	0	1	1	0	0	0	0	1	
Scan	0	0	1	1	0	0	0	1	1	(Keyboard scanning may resume)
Mouse	0	0	1	1	0	0	1	0	1	(More mouse changes may be queued)

Reset sequencing

Direction	Code	Expected reply	Action on wrong reply (Sender)	Action on timeout (Sender)	Action if unexpected (Receiver)
ARM -> Kb	Hard reset	Hard reset	Resend	Resend	Hard reset
Kb -> ARM	Hard reset	Reset Ack 1	Resend	Nothing	Hard reset
ARM -> Kb	Reset Ack 1	Reset Ack 1	Hard reset	Hard reset	Hard reset
Kb -> ARM	Reset Ack 1	Reset Ack 2	Nothing	Nothing	Hard reset
ARM -> Kb	Reset Ack 2	Reset Ack 2	Hard reset	Hard reset	Hard reset
Kb -> ARM	Reset Ack 2	Ack Scan	Nothing	Nothing	Hard reset

17. Appendix B The A500 Keyboard

The keyboard interface allows different keyboards to be attached via a duplex serial link upto a maximum length of 3 metres using good quality BT six core cable. The keyboard contains 97 keys, a mouse interface, a loudspeaker and 2 software protection devices.

17.1 Keyboard Hardware Description

The keyboard contains a 10 by 10 matrix allowing for up to 100 keys with 2 key roll-over. In addition, 4 shifting keys are provided: two SHIFT keys which are wired in parallel, a CMD key, and a LOOKS key. A caps-lock LED is incorporated in the caps-lock key. The mouse interface will support up to 3 mouse keys with infinite roll-over. The keyboard is controlled by a single-chip micro, and has a regulator on board to derive the +5v rail from a +12v input- A reset button is situated on the rear of the keyboard whose function is to reset the keyboard and the main machine. The keyboard contains its own power-on reset circuitry and may be un-plugged and re-plugged without reseting the main machine.

All the main functions of the keyboard are controlled by a 6500/11 micro IC1, with on-chip firmware. The micro drives the columns of the keyboard matrix with 4 output lines, which arc decoded by IC2, a 74LS145. The matrix rows are then read by the micro directly. The shifting keys, SPD's, and mouse all interface directly with the miero. The caps-lock key is driven by a pair of inverters connected in parallel (IC3). The serial line to the main machine is buffered by 1C3. SW1 is the reset switch. One pair of contacts resets the main machine, the other set resets the 6500/11 via IC3. A power-up reset is also provided. Provision is made on the PCB for fitting the optional components required to prevent RFI being radiated from the keyboard serial link. In order to accommodate possible variations in the mouse interface connections the mouse connector is wired via a 20 way DIL. socket. This socket is tracked across so that no component need be fitted if the 'standard' connection is used. These tracks can be cut and a wired header fitted to tailor the interface as required. Two SPD's are catered for. SPD1 is the user' s key and plugs into PL2 from outside the keyboard. A 24 way DIL area is provided on the PCB so that another SPD, SPD2, can be plugged in or soldered internally. These SPD's are wired in parallel except for their outputs which go to separate pins on the 6500/11. Thus 2 levels of protection are possible.

17.2 6500/11 Port Map

PA0 SPD2 din	PB0 Mouse X	PC0 Row 0	PD0 Col b0
1 SPD1 din	1 House X'	1 Row 1	1 Col b1
2 SHIFT keys	2 Mouse Y	2 Row 2	2 Col b2
3 LOOKS key	3 Mouse Y'	3 Row 3	3 Col b3
4 CMD key	4 Mouse key 1	4 Row 4	4 SPD1,2 reset
5 Mouse key 2	5 Mouse key 0	5 Row 5	S SPD1,2 dout
6 Serial out	6 Row 8	6 Row 6	6 SPD1,2 clock
7 Serial In	7 Row 9	7 Row 7	7 Caps-lock LED

17.3 Notes

(1) The 6500/11 has internal pull-up resistors (value 6K -50% +100%) on PA, PB, PC.

(2) All key inputs are 0 when the key is pressed.

(3) To drive the key matrix, a number is written to PD0-3 (PD0 = LSB)- This is decoded to drive a unique matrix column- Numbers written to PD map directly onto column numbers, ie. writing 3 to

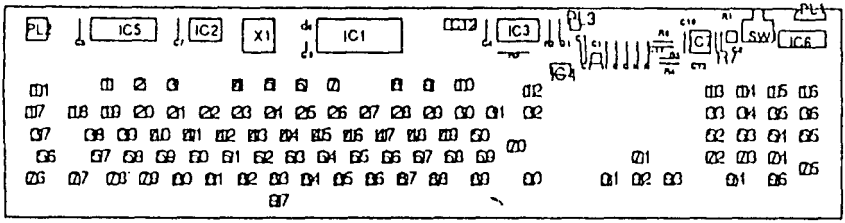


Figure 21: A500 keyboard PCB

PD0-3 drives column number 3 LOW. Other columns remain HIGH

(4) Writing a "1" to PD7 wili illuminate the Caps-lock LED.

(5) The 6500/11 mask option chosen does a /2 on the clock crystal frequency giving a 1 MHz interal clock. Since the transmit and receive data rates are one sixteenth of the counter A interval timer rate, counter A should be loaded with 00- This gives a 31.25 Kbit data rate-

17.4 Key Matrix to Key Number

		ROWS								
		0	1	2	3	4	5	6	7	8	9
	0	2	3	4	6	13	12	16	15	8	10
	1	1	21	22	5	33	31	36	14	7	9
C	2	20	41	23	24	52	30		35	26	28
O	3	38	79	62	83	91	68		73	65	67
L	4	76	80	82	97	96	90		75	86	88
U	5	56	78	81	84	92	70		74	85	87
M	6	19	39	43	44	72	50		54	46	48
N	7	11	40	42	25	71	32		34	27	29
	8	17	58	60	63	93	69		55	64	66
	9	18	59	61	45	94			53	47	49

17.5 Keyboard Links Connectors and Test Points

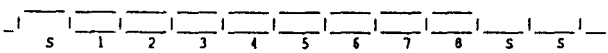
17.6 Keyboard connector (PL4):

The connection provided on die keyboard will be by means of 6 fast-on 0,110 tabs. An extra 0v tab (7) is also provided in this group. The pin connections are as follows:

pin	Function
1	data out of keyboard
2	reset
3	data in to keyboard
4	0v
5	audio
6	+12v
7	0v

17.6.1 Pins 1 and 3: Data

This is the serial data line. 8 bit packets are exchanged with 1 start bit and 2 stop bits as shown.



The convention for the data bits is:

0v : 1
+5v : 0

No flow control is provided for the data packets. The data rate is fixed at 62.5 Kbits/s. No parity error checking is done.

17.6.2 Pin 2: Reset

This is the hardware reset signal from the keyboard to the "A" machine. It is active low.

17.6.3 Pin 4: Power

0v earth return for power, data, and audio signals.

17.6.4 Pin 5: Audio

High level audio signal to drive the loudspeaker amplifier which in turn drives an 8 ohm loudspeaker. Earlier designs drove a 300 ohm speaker directly but this proved a difficult part to source.

17.6.5 Pin 6: Power

+12v power.

17.6.6 Pin 7: Power

0v connection. A flying lead is connected from here to a stud on the keyboard case

17.7 Mouse connector (PL1):

This is a 9 way subminiature 0-Type Socket

Pin	Function
1	+5v power for mouse
2	X'
3	X
4	Y
5	Y'
6	KEY 0
7	KEY 1
8	KEY 2
9	0v

17.8 SPD1 connector (PL2):

This is a BT 600 type 6 way socket.

Pin	Function
1	+5v power
2	data in
3	clock
4	reset
5	data out
6	0v

17.9 Keyboard PCB Parts

17.9.1 Integrated Circuits

IC1	6500/11	40 pin
IC2	74LS145	16 pin
IC3	74HCTI4	14 pin
1C4	LM7805CT or LM340T-5.0	
IC5	SPD2	24 pin (not fitted)
IC6	header	20 pin (not fitted)
IC7	LM386	

17.9.2 Resistors

R1	100R
R2	10K
R3	330R
R4	1K
R5	56R
R6	10R
R7	10K (not fitted)

17.9.3 Diodes

D1	IN4148
D2	LED in caps lock key

17.9.4 Crystals

X1	2MHz crystal

17.9.5 Capacitors

C1	10uF 16v
C2	220nF
C3	470nF
C4-C7	33nF
C8	10uF 16v
C9	22pF
C10	33nF
C11	47nF
C12	470uF 6.3V (Farnell 031 33471)
C13	47nF (not fitted)

17.9.6 Sockets

PL1	9 way sub-miniature right-angled PCB mounting D-type socket
PL2	PCB mounting BT socket. BICC-VERO ?????
PL3	2 molex pins
PL4	

17.9.7 Misc

SW1	2 pole change-over switch. CK 8225A or EMS 8024L.
11-15	1uH choke (not fitted)
SP1	8R speaker
SK1	2 way molex socket 2 inserts for above 2 way cable A/R for above

18. Appendix C Key Number to Legend

No.	PART No.	LEGEND
I	JN-Y038	F1
2	JN-Y039	F2
3	JN-Y040	F3
4	JN-Y041	F4
S	JN-Y042	F5
6	JN-Y043	F6
7	JN-Y044	F7
8	JN-Y045	F8
9	JN-Y046	F9
10	JN-Y047	FI0
11		NO LEGEND
12		NO LEGEND
13		NO LEGEND
14		NO LEGEND
15	JN-F001	/
16	JN-F002	*
17		NO LEGEND
18		NO LEGEND
19	JN-Q001	1 !
20	JN-Q050	2 "
21	JN-Q003	3
22	JN-Q004	4 $
23	JN-Q005	5 %
24	JN-Q051	6 &
25	JN-Q052	7 '
26	JN-Q053	8 (
27	JN-Q054	9)
28	JN-Q055	0
29	JN-Q056	- =
30	JN-Q057	^ -
31		NO LEGEND
32		NO LEGEND
33		NO LEGEND
34		NO LEGEND
35		NO LEGEND
36	JN-F004	-
37		NO LEGEND
38	JN-Y008	TAB
39	JN-Q014	Q
40	JN-Q015	W
41	JN-Q014	E
42	JN-Q017	R
43	JN-Q018	T
44	JN-Q019	Y
45	JN-Q020	U
46	JN-Q021	I
47	JN-Q022	O
48	JN-Q023	P
49	JN-Q059	@ '
SO	JN-Q024	{ [
51	(Not fitted)	
52		NO LEGEND
53		NO LEGEND
54		NO LEGEND
SS		NO LEGEND

56		NO LEGEND
57		NO LEGEND
58	JN-Q026	A
59	JN-Q027	S
60	JN-Q028	D
61	JN-Q029	F
62	JN-Q030	G
63	JN-Q031	H
64	JN-Q032	J
65	JN-Q033	K
66	JN-Q034	L
67	JN-Q060	; +
68	JN-Q061	: *
6)	JN-Q025	] }
70		
71	JN-F016	(UP ARROW)
72	J(1-E001	1
13	JN-E002	2
74	JN-E003	3
7S	JN-D014	ENTER
76		NO LEGEND
77	JN-Y009	SHIFT
78	JN-Q144	\ |
79	JN-Q038	Z
80	JN-Q039	X
81	JN-Q040	C
82	JN-Q041	V
83	JN-Q042	B
84	JN-Q043	N
85	JN-Q044	M
86	JN-Q045	, <
87	JN-Q046	. >
88	JN-Q047	/ ?
89	JN-Y049	SHIFT
90		NO LEGEND
91	JN-F011	(LEFT ARROW)
92	JN-F010	(DOWN ARROW)
93	JN-F012	(RIGHT ARROW)
94		NO LEGEND
95	(Not fitted)	
96		NO LEGEND
97		NO LEGEND
98	(Not fitted)	
99	(Not fitted(	
100	(Not fitted)	

19. Appendix D Podules

19.1 Device Drivers and the Podule Manager

Since the physical address of a podule depends on which slot it has been plugged into its driver software must be informed, or be able to determine. its actual address. To achieve this every class of podule must have a unique number which can be read by the podule manager which may intern bind podule device drivers with their podules. A single device driver may control many podules but a podule may only be assigned to a single driver.

19.2 Simple Podules

These podule occupy an address space decoded by LA[14:15] and LA[13]. LA[13] controls the selection of Podule data registers and the Podule Identity space. Each Podule can address a 4Kbyte space.

19.3 Memc Podules

These are Podules that attatch directly to the MEMC IOAK/IOGT interface. A maximum of four of these Podule may be attatched to an A500. The IO address space is split into two; the upper half with LA[21]=1 is occupie by IOC. The lower half is decoded into four identical spaces by LA[14:15]. This wastes the space LA[16:20] and is done to reduce the signal count. Each Podule can then address an 8KByte space decoded by LA[2:13].

19.4 Co-Processor Podules

One of the podule slots is nearly tracked to allow a Co-Processor to be attitched.

19.5 Software Requirements

TRICKY

19.6 Hardware Requirements

All podules must implement the Podule Identification protocol. A podule may only present two HC or HCT load per signal. Podules may only be added with the power OFF.

19.7 Podule Identification

The PODULE IDENTITY (PI) is read by an IOC TYPE 0 READ of address 0 of the Podule Identity space. If Podule Select PS and I/D (LA[13]) are both low then the low byte of the Podule Identity must be placed on BD[0:7).

19.7.1 Identification Extension

If the Podule Identity read from address 0 is 0 then the Podule Identity is extended. This is yet to be defined but I expect the podule will provide a 64bit podule number and several optional user bytes like the serial number date of manufacture from a byte wide PROM at incrementing addresses.

0	IRQ request
1	Present Must be driven low
2-7	ID

IF ID-0 THEN extended ID to be read

19.8 Podule Presence

Bit BD1 has a weak pullup on the main system board. If no podule is present at the addressed location this bit will be read as "1". A podule must drive BD[0:7] if its Podule Select Line is LOW and the Identity/Data line is LOW.

19.9 Interrupts

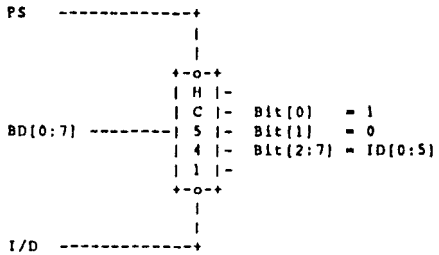
Podules are allowed to generate both ARM IRQ's and FIQ's though not directly. Them are two open-drain busses PIRQ and PFIQ which are individually masked through IOC. No hardware support is provided for PFIQ servicing.

19.9.1 Podule IRQ

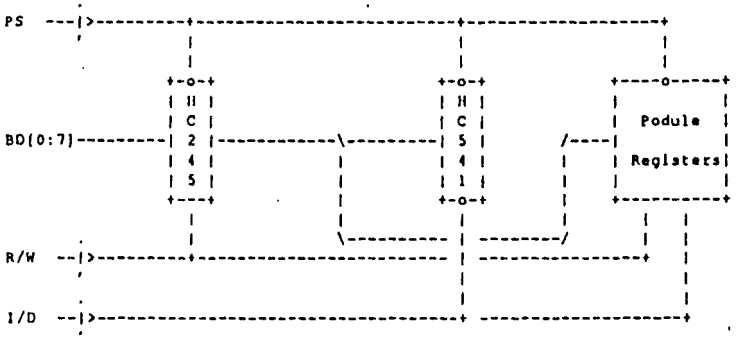
To assist PIRQ servicing every podule must indicate in Bit 0 of the Podule Identity Word 0 whether it is requesting a PIRQ. This allows the podule manager to poll the podules efficiently to determine which podule driver should be called. The order in which the podules are tested for PIRQ requests is the only observable diffence between podule slots.

19.10 Examples

19.10.1 Minimum Identification



19.10.2 Simple Podule Example



Pin	a	b	c (Backplane)	c (Podule)			
32	V5	.	V12	V12			
31	BD[0]	.	reserved	reserved			
30	BD[1]	.	V5	V5			
29	BD[2]	.	REF8M	REF8M			
28	BD[3]	.	CLK8	CLK8			
27	BD[4]	.	CLK2	CLK2			
26	BD[5]	.	reserved	reserved			
25	BD[6]	.	BL	BL			
24	BD[7]	.	IORQ	IORQ			
23	BD[8]	.	IOGT	IOGT			
22	BD[9]	.	S[4]	PS			
21	BD[10]	.	S[7]	S[7]			
20	BD[11]	.	C0	C0			
19	BD[12]	.	C1	C1			
18	BD[13]	.	EFIQ	EFIQ			
17	BD[14]	.	PFIQ	PFIQ			
16	BD[15]	.	PIRQ	PIRQ			
15	LA[2]	.	PRE	PRE			
14	LA[3]	.	PWE	PWE			
13	LA[4]	.	PR/NW	PR/NW			
12	LA[5]	.	RST	RST			
11	LA[6]	.	HS3	HS3	reserved	Winni	Podule
10	LA[7]	.	S508	S508	"	"	"
9	LA[8]	.	S500	S500	"	"	"
8	LA[9]	.	WDRQ	WDRQ	"	"	"
7	LA[10]	.	WIRQ	WIRQ	"	"	"
6	LA[11]	.	LA[21]	MS			
5	LA[12]	.	AGND	AGND			
4	LA[13]	.	AOUT	AOUT			
3	LA[14]	.	AIN	AIN			
2	LA[15]	.	V-5	V-5			
1	V0	.	V0	V0			

19.11 Signal Explanations

BD[0:15]	Buffered IO Data BUS
LA[2:15]	Latched IO Address BUS
AIN	Analouge BUS Input
AOUT	Analouge BUS Ouput
AGND	Analouge BUS Ground
MS	Module Select
CPA	?
CPU	?
CPI	?
OPC	?
PHHB	?
RST	IO BUS Reset Line
LRW	HIGH indicates a READ a LOW WRITE
WE	Podule Write strobe
RE	Podule Read strobe
PIRQ	Podule open-drain IRQ bus
PFIQ	Podule open-drain FIQ bus
FH2	Reserved for ACORN use
C1	12c SCL
C0	12c SDA
PS	Podule Select
S[6]	Reserved for ACORN use
IOGT	MEMC IO interface control
IOAK	MEMC IO interface control
BL	MEMC IO interface control
CLK2	2 MHz syncronous clock
CLK8	8 MHz syncronous clock
M8REF	System clock use with care
CLK24	.Master clock
VS	5 Volts
V12	12 Volts
V-5	-5 Volts
V0	0 Volts