# MASTER SERIES HARDWARE SPECIFICATION

## INTRODUCTION

The Master Microcomputer consists of a central processing unit with associated memory and various input/output devices for communication with external equipment. Only a fully configured system will be described here although reference to sub-systems will be made where relevent.

### The Core Machine

All input/output (I/O) computing is performed by a 65C12 CPU with its principal ancillary components:-

128K byte of Dynamic Random Access memory:- Special expansion options allow a further expansion of 64 Kbyte. Dedicated hardware can be used to expand this almost indefinitely.

262K byte of Read Only Memory:- Special expansion options allow a further expansion of approximately 1/2 M byte of ROM. Plug in cartridges are available which accept up to 256K byte of ROM.

### Internal I/O

Various I/O devices operate solely within the confines of the system to either improve facilities or increase throughput. These are as follows:-

6522 VIA devices - Two of these are provided; one of which interfaces to:-

A 93 contact keyboard with 2 key rollover.

3-Channel sound generator with additional noise channel. Battery backed up Real-Time Clock and fifty bytes of RAM. Co-Processors.
These consists of an additional CPU with associated memory. They has no I/O capability of their own and depend entirely on the main processor to supply such information. They do all the computation not associated with I/O operations.

When a co-processor is not fitted, the main processor has to perform both I/O and non I/O computation.

External I/O

Video display:- A 6845 CRT controller is provided to format the output from RGB, composite video and PAL/NTSC connectors.

Analogue to Digital Converter:- A four channel converter provides 10 bit binary conversions in 5ms. The absolute accuracy will depend on the conditions of use.

Tape Interface:- Facilities to both save and retrieve data from audio cassettes is provided.

Disc Interface:- Facilities to both save and retrieve data from standard Shugart connected media. Filing systems are provided to support data encoded in FM of MFM.

Network Interface:- Connection to the ECONET is provided by a 68B54 advanced data link controller. This is fitted on a daughter board and may as such be fitted as an optional extra.

1MHz Bus:- The standard BBC computer 1MHz bus is provided.

External Second Processor:- An external second processor may be connected. Selection of either internal co-processor - or external second processor is performed by software. Only one second or co-processor can be active at a time.

Centronics Printer Port:- Connection is provided for the standard parallel printer port configuration.

User Port:- The user port is an eight bit bidirectional bus with two extra handshaking/serial lines. These are unbuffered.

RS423:- A serial RS423 port is provided.

Audio Output:- The output from the sound generator is amplified to a speaker and provided at a phono style connector. Sound transfer to and from the modem is provided.

Modem:- Connection for a modem with both dial pulse and dual tone multi-frequency dialing is provided. This facility is provided to support third party hardware.

CORE MACHINE

Operation of the RAM and ROM is controlled by the Memory Controller integrated circuit. The principal function of this device is to control the memory paging structure.

Memory Map

The 65C12 can directly address 64K locations. As over 1/2 Mbyte may be resident (depending on the users configuration), a paging scheme is implemented to allow access to it.

The basic memory assignment is as follows:

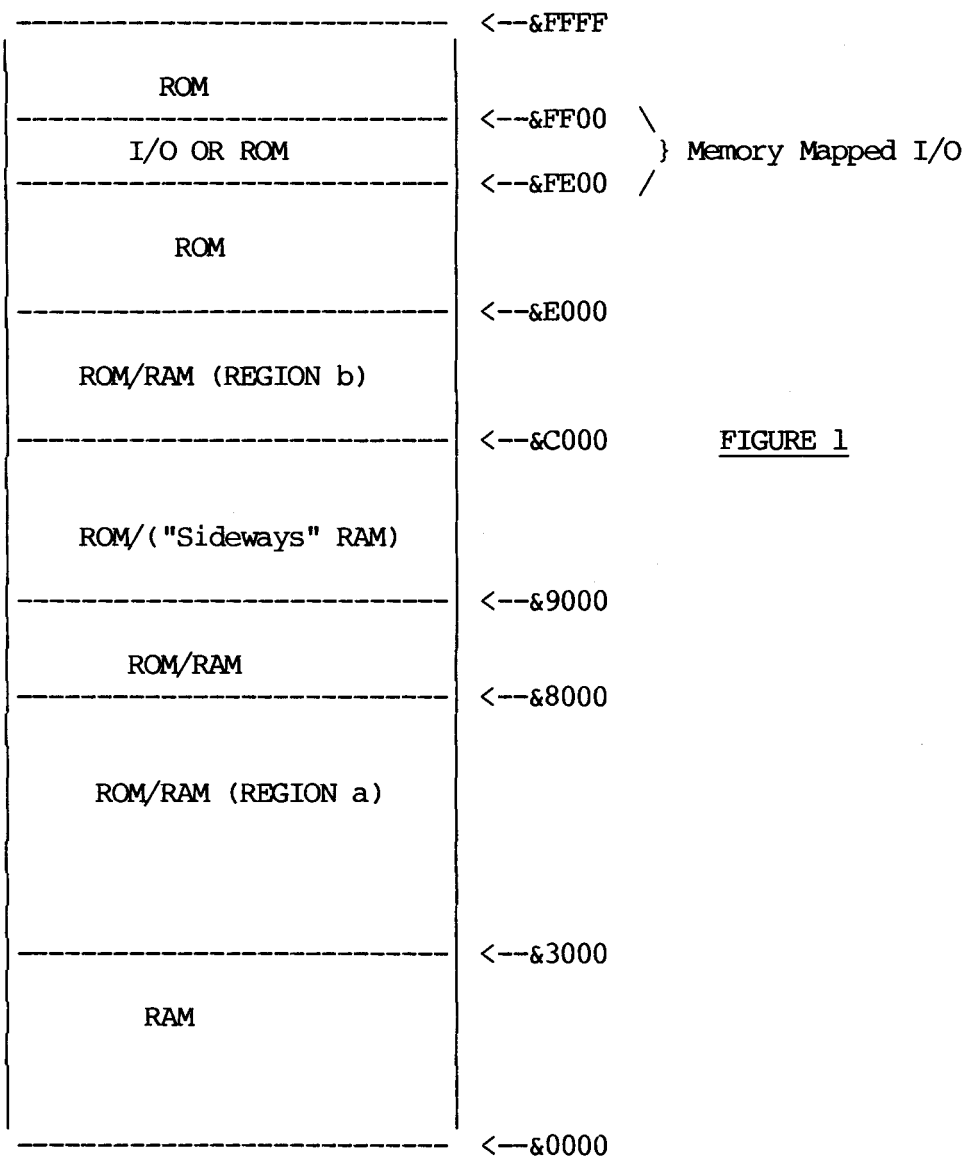



FIGURE 1

The current memory map is dictated by the contents of the two latches, ROM SELect and ACCess CONtrol located at &FE30 and &FE34 respectively.

The contents of these two latches are as follows:-

| | d7 | d6 | d5 | d4 | d3 | d2 | dl | d0 |
|---|---|---|---|---|---|---|---|---|
| (&FE30) | RAM | 0 | 0 | 0 | PM3 | PM2 | PM1 | PM0 |
| (&FE34) | IRR | TST | IFJ | ITU | Y | X | E | D |

The contents of ROMSEL dictate the selection of memory which resides from &8000 to &BFFF.

ACCCON

The contents of ACCCON principally dictate the activity of two regions of memory:

(a) &3000 to &7FFF
(b) &C000 to &DFFF

128Kbyte RAM

The RAM is functionally split up into two regions: The main region supports the language workspaces, buffers etc. and provides the bit mapped screen. The second region provides 4, 16k "Sideways" RAM segments. These are link selected into ROM locations 4,5,6 and 7. They may be deselected, reinstating the ROM sockets in "chunks" of 32K byte.

Within the main 64K byte region, the lower 32k is used wthin the &0000 to &7FFF region of the CPU memory map, as shown in figure 1.

The upper 32k is split up into three, self-contiguous regions. The largest portion of this is a 20k byte region designated LYNNE. This can be overlayed on the region (a) of main memory.

* When bit D in ACCCON is set, the CRT controller will display the contents of LYNNE. When bit D is cleared, the region (a) of main memory will be displayed.

* When bit E in ACCCON is set, if the address range is &3000 to &7FFF the CPU will read/write Lynne according to the flow shown in figure 2.

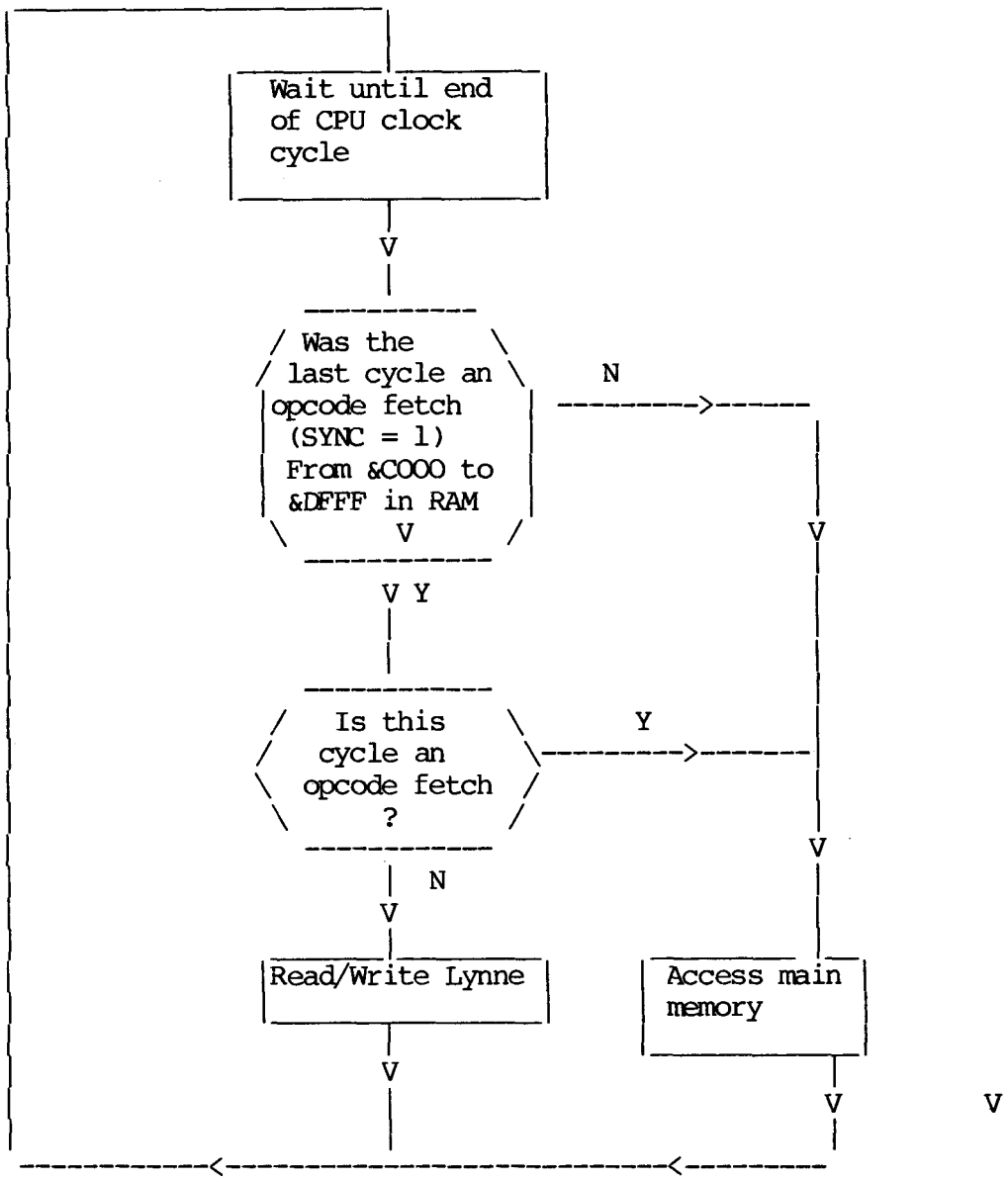



FIGURE 2

This system allows for the screen bit map to be removed from the main CPU memory map, of which it occupies a significant proportion. It will, however, only work if the screen is being accessed by opcodes from a known region - i.e. the MOS VDU drivers. A mechanism also is provided to permit 'illegal' screen access:

* Bit X in ACCCON, when set, causes all accesses to region ( a) to be re-directed to LYNNE. This occurs irrespective of the opcode address, hence considerable care will have to be exercised in its use. When cleared, the memory map returns to its usual format.

In the same way that the Basic variable HIMEM will always have the value &8000 when LYNNE is used, ,it is desirable for the variable PAGE to have the value &E00, irrespective of the current filing system.

This is achieved by providing a filing system workspace as follows:-

* Bit Y in ACCCON when set, cause 8K byte of RAM referred to as HAZEL to be overlayed on the MOS VDU drivers, ie from &C000 to &DFFF.

Clearly, when this bit has been set, no calls may be made to the MOS for VDU operation. The code which performs this paging operation is responsible for resetting the Y bit, as no hardware is provided for this purpose.

The remaining bits in ACCCON are used to control various peripheral systems:-

* The bit ITU in ACCCON when set enables the CPU to accesss the internal second processor rather than the external one.

* The bit IRR in ACCCON is InterRupt Request. When set, this bit causes an open drain output to pull the CPU NIRQ pin down to Vss.

ROMSEL

The contents of ROMSEL determine the paging of memory in the 16K region &8000 to &BFFF. One of Sixteen, unique 16K byte ROM memory segments may be selected. One additional 4K byte RAM segment may be selected from &8000 to &8FFF.

Eight of the segments are assumed to be in 4, 32K byte ROMs where the least significant bit of ROMSEL selects between the upper and lower segments. Seven of the segments exist together with a ROM which is active from &C000 to &FFFF, within a 128K byte ROM. This ROM is connected via a separate data bus. The 4,32K byte devices and one, 16k byte device are connected in a matrixing scheme as shown in figure 3.

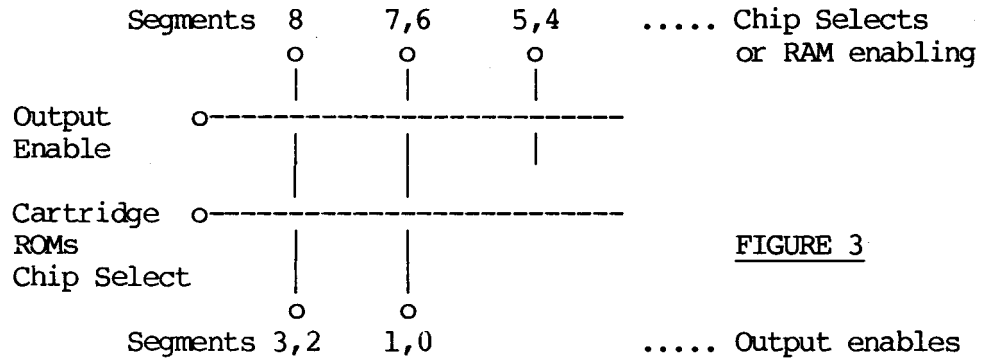



FIGURE 3

In this way, fewer connections to the controller logic are required to select a given ROM, although the power dissipation will be increased if all the ROMs in one column are inserted.

A chip select will be driven low if an access to one of the segments (4 to 8) is required. If a cartridge ROM is required, then the Cartridge ROM chip select will be driven high. All chip selects are a decode of the CPU address most significant nibble.

An output enable is turned active low during the CPU phi2 period depending on which segment is required.

The segment to be selected is determined by the binary number held within the lease significant nibble of ROMSEL.

Overlaid RAM in ROM area

When the bit RAM is set in ROMSEL, accesses to the region &8000 to &8FFF are redirected from the currently selected ROM to a region of RAM referred to as ANDY. It is the responsibility of the code which set RAM to clear it after accessing ANDY. This is necessary to ensure correct operation of software in ROM.

Summary of RAM memory map

The 64K of DRAM is distributed as follows:-

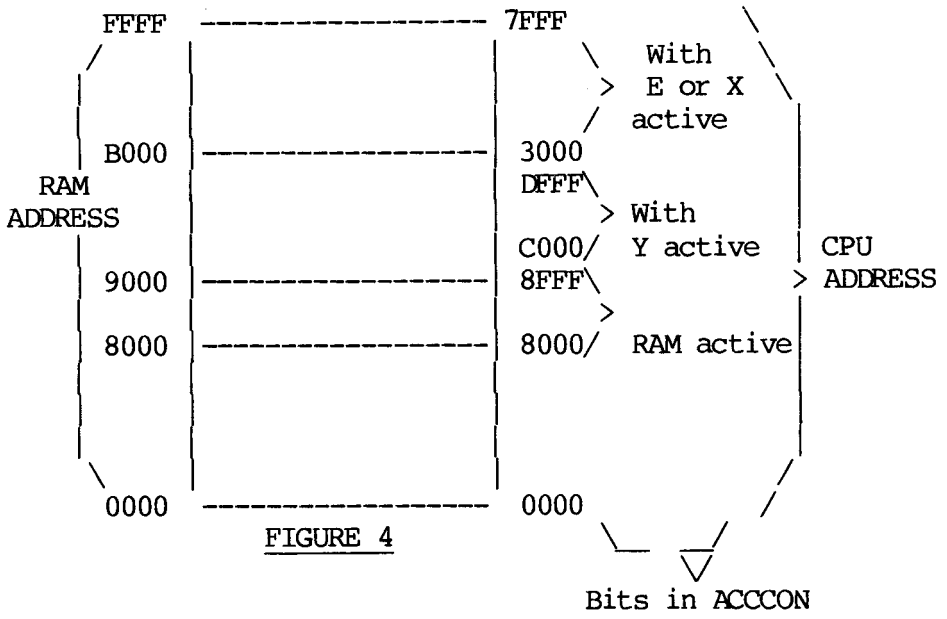



FIGURE 4

A further 64k byte of RAM is available as 4 pages of 16K byte from &8000 to &BFFF. The ROM slots 4,5,6 and 7 are not active when this RAM is link selected to be active.

INTERNAL I/O

Slow peripherals:- These are subsystems which are provided with data from port A of the system VIA. This data is stable until next programmed by the CPU.

Keyboard

General description:- 93 keys are provided. 92 of these are in a modified 8 x 13 matrix as shown in figure 5. A device VOOIGC is used to scan the keyboard. During idle (free run) mode, pressing any key will cause an IRQ to be generated via the system 6522. A connection is provided from VOOIGC to a 6522 ' CA' type connection. Hence the interrupts thus generated are controlled by the 6522 control register. Depression of either of the shift keys, or the control key does not cause an interrupt to occur.

Keys are arranged as a QWERTY style keyboard with extra keys for a numeric keypad. Ten additional 'function keys' together with cursor control buttons, etc, are provided.

The "BREAK" key will reset the CPU and abort any access to the clock/RAM chip. To prevent accidental operation, a mechanical lock is provided. This is a plastic cam which is rotated through 90 degrees to stop the keytop from being depressed.

Keyboard Operation:- During free run mode, the keyboard column lines are continually scanned by incrementing a counter, decoding its outputs and pulling low a column line. Any key depressed will cause the interrupt to be generated. A signal, KeyBoard ENable is generated to stop free running mode. The counter contents are now loaded by CPU operation to determine on which row the key was pressed. The rows are then individually selected to determine which key was pressed.

The VOOIGC is supplied with data from the slow data bus:-

PA0 to PA6:- These are the slow bus connections. PA0 to PA3 are the column select inputs and PA4 to PA6 are the row select inputs. PA7 is a three state connection which is driven active low when a row/column combination describes a depressed key.

R0 to R7:- The keyboard row input connections are normally held high by internal pull-up resistors. If a key is depressed it will cause the appropriate row connection to be pulled low when its column is selected.

C0 to C14:- These open collector column driving outputs are sequentially taken active low in auto scan mode at a rate of 1MHz. In polled mode (nKBEN active low) the slow bus inputs PA0 to PA3 determine which output will be low. The selected column output is a direct decode of these inputs.

CA2:- Connected to the system VIA, this output will cause the VIA to generate an nIRQ. The line will be active low when an active key is detected.

nKBEN:- Generated by the system VIA, this line is taken active low to enable the row and column addresses to be determined by the Operating System.

MHz1:- This is the timing reference.SWT1

, RST0:- These connections are not used.

The Keyboard Matrix

The keys are physically arranged as a QWERTY type keyboard with 10 function keys, 4 cursor control keys and a 19 key numeric keypad.

The matrix is as follows:-

| | C0 | C1 | C2 | C3 | C4 | C5 | C6 | C7 | C8 | C9 | C10 | C11 | C12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R0 | ESC | f1 | f2 | f3 | f5 | f6 | f8 | f9 | \| | @ | 4' | 5' | 2' |
| | | | | | | | < | > | ? | | | | |
| R1 | TAB | Z | sp | V | B | M | , | . | / | copy | 0' | 1' | 3' |
| | | | | | | | | + | } | | | | |
| R2 | SHIFT LOCK | S | C | G | H | N | L | ; | ] | del | #' | *' | ,' |
| | | | | | | | | | * | | | | |
| R3 | CAPS LOCK | A | X | F | Y | J | K | @ | : | ret | /' | del' | .' |
| | ! | " | | | & | | | | { | | | | |
| R4 | 1 | 2 | D | R | 6 | U | O | P | [ | @ | +' | -' | ret' |
| | | | | | ' | | ) | | £ | | | | |
| R5 | f0 | W | E | T | 7 | I | 9 | 0 | _ | @ | 8' | 9' | |
| | | # | $ | % | | ( | | = | ~ | | | | |
| R6 | Q | 3 | 4 | 5 | f4 | 8 | f7 | - | ^ | @ | 6' | 7' | |
| R7 | SHIFT | CTRL | | | | | | | | | | | |

FIGURE 5

Sound Generator

The sound generator is an SN7694A device. Three sound channels plus one pseudo random noise channel are provided. The full description of it is found in the manufacturers data sheet. It is provided with a reference clock of 4MHz from central timing. The output is filtered as described in the section 'Audio Circuitry'.

The output can also be connected by screened cable to the optional modem. This output is mixed on the modem board to generate dialling tones for DTMF exchanges where the modem hardware does not provide such tones itself.

Real time clock with

RAM Battery back-up

A 146818 RTC and RAM chip is provided with battery backed supply. The chip operation is described in the manufacturers data sheet. In its fully charged state, the internal lithium battery will provide over one year of back up power. Alternatively, components may be fitted to the circuit board which provide the switching of a rechargeable battery on the keyboard. This battery, like its support components are not fitted as standard. If these are fitted by the user, the warrantly will be invalidated.

The keyboard mounted battery is charged whilst the computer is running from the mains supply. The proportion of charge accummulated during operation is shown in figure 6 for an initially flat battery. This is an approximation dependant on conditions of use, as the actual charge accumulated will vary with temperature and duty cycle (i.e. ratio of time on charge, to tine on discharge).

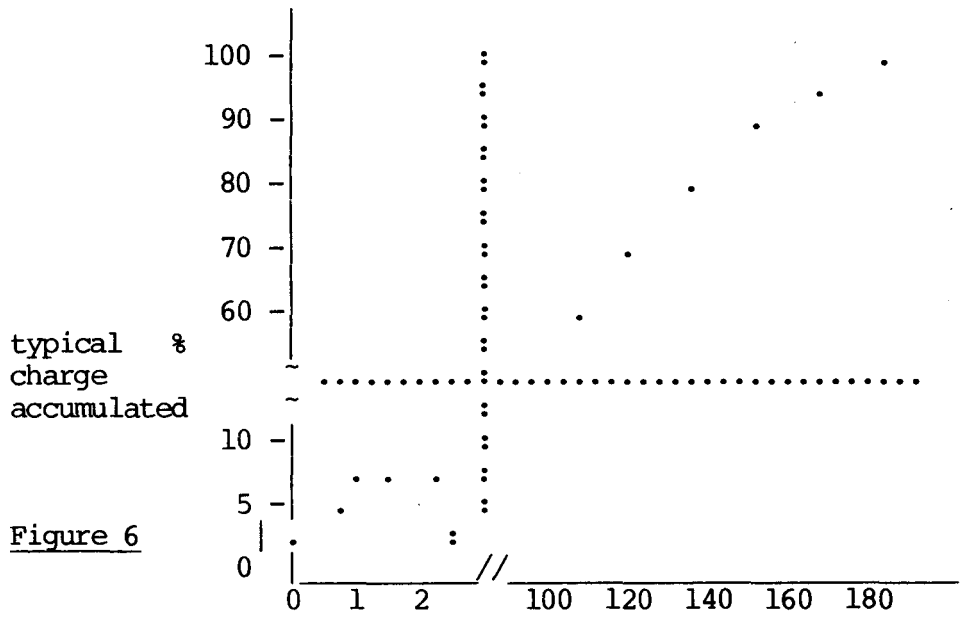



Figure 6

An over-charge prevention circuit is provided with the following action:

a) Upon switch on, charging current of about 30mA is applied.

b) After approximately 15 minutes the charging current falls to 1mA.

c) "Trickle" charging continues at 1mA for as long as mains power is applied.

The minimum charge burst is designed to provide battery back-up over a weekend after just a few minutes operation.

A 10uf capacitor is connected across the clock chip supply connections. This is to prevent loss of data in the event of accidental battery disconnection.

Configuration Status:- Fifty bytes of CMOS RAM are available within the chip. Twenty of these are used by the operating and filing systems for initial configuration of the hardware. Of the remainder, ten are reserved for future use by ACORN, ten are for 'Third Party' use and the remainder are for the user.

Clock:- The clock operates from a 32.768KHz crystal oscillator. A trimming capacitor is provided as is a test point with the buffered clock output. Year, month, day, hour, minute and second information is provided with automatic leap year (but not automatic leap century) correction. An alarm is also included within the chip, but operating system support to this facility is not provided. An optional nIRQ connection can be made to the CPU from the clock chip, enabling the alarm to change program flow. Operation of the clock chip in this manner involves direct manipulation of the chip control signals and should only be attempted by competent programmers. Acorn Computers are not responsible for incorrect programming by the user/software supplier.

If power is removed during an access to this chip, the chip select will become invalid. This cannot however remove the possibility of write accesses being corrupted. This is done by inverting the chip select with a transistor whose collector resistor is connected to the battery backed supply. As power fails to the main circuitry, the transistor base current reduces and the transistor switches off deselecting the chip.

1 MHz Internal I0:- Various devices operate at a 1MHz bus rate. Only one internal I/O component works at this speed - the system VIA.

System VIA:- A 6522 allows several sources to create maskable interrupts. The sources are:-

a) CRTC vertical synchronisation.
b) A-D converter; end of conversion signal.
c) CRTC light pen strobe.
d) Keyboard key detect.

It also provides the previously mentioned slow data bus.

Port B on this device generates and reads a number of internal hardware strobes. These are as follows:-

| Port B Data | Strobe | Active Level |
|---|---|---|
| D7 D0 | | |
| D X X X X X X X | Clock Address | H |
| X D X X X X X X | Clock chip enable | H |
| X X D X X X X X | 'Fire' button 1 | Input |
| X X X D X X X X | 'Fire' button 2 | Input |
| X X X X D 0 0 0 | Sound chip select | L |
| X X X X D 0 0 1 | Clock R/W | L |
| X X X X D 0 1 0 | Clock Data | Q |
| X X X X D 0 1 1 | Keyboard enable | Q |
| X X X X D 1 0 0 | C0 } Screen control | L |
| X X X X D 1 0 1 | Cl } Signals | H |
| X X X X D 1 1 0 | Caps Lock indicator | L |
| X X X X D 1 1 1 | Shift Lock indicator | L |

Note: Q is the value of D after the port write operation is completed

2MHz Internal I/0:- Only one internal I/0 component operates at this speed - the internal second processor TUBE. Its data bus is connected directly to the CPU data bus.

The second processor interface will only be specified as a hardware data transfer definition. In this way, the actual second processor used will not be constrained by this specification.

This is a parallel port providing the following data access signals:-

i) D0 to D7 .... A bi-directional bus to TTL levels.
ii) A0 to *A2* .... A uni-directional bus to CMOS levels.

The following control and timing signals are provided:-

i) Host CPU phi2 .... CMOS levels
ii) System Reset .... TTL levels
iii) Host CPU nIRQ .... This must be an 'open collector' node with an active low TTL level
iv) 8MHz timing reference .... TTL levels
v) TUBE chip select CMOS levels
vi) Read/Write TTL levels

EXTERNAL I/O

1MHz External I/0:-

Screen Output:- There are two chips primarily responsible for providing the screen output:-

a) 6845

b) Acorn proprietary VIDPROC

High Resolution Modes:- The 6845 generates a linear memory address sequence which increments every 0.5 us or lus, depending on the video bandwidth selected and video data format.

The amount of memory reserved for screen use is also varied. The available options are shown on the next page:

Figure 7 - Video Data Formats

| "Mode" | Format Pixels/Byte | Reserved Memory Bytes | |
|---|---|---|---|
| 0 | 8 | 20K | |
| 1 | 4 | 20K | |
| 2 | 2 | 20K | |
| 3 | 8 | 16K | |
| 4 | 8 | 10K | |
| 5 | 4 | 10K | |
| 6 | 8 | 8K | |
| 7 | Teletext | 1K | |
| 128 | 8 | 20K \ | |
| 129 | 4 | 20K \| | |
| 130 | 2 | 20K.\| | Reserved |
| 131 | 8 | 20K > | in |
| 132 | 8 | 20K \| | LYNNE |
| 133 | 4 | 20K \| | |
| 134 | 8 | 20K \| | |
| 135 | Teletext | 20K / | |

All modes except 7 and 135 display a bit mapped image of the reserved memory. The 6845 may be re-programmed to display any arbitary section of memory. If this is done, however, the hardware scrolling will not work correctly, as it assumes that the screen memory is in its usual location. The screen always ends at &7FFF and starts 1,8,10 or 20K further down than that, depending on the selected mode.

The selection of video bandwidth and data format is performed by programming the VIDPROC. The cursor size and position is also controllable by VIDPROC. Special measures have been taken to ensure correct cursor operation in the Teletext modes.

Teletext

The Teletext modes do not generate a bit mapped display, but a character cell one. The character/graphics ROM within a SAA5050 device generates RGB signals according to the desired character/graphics information within the reserved memory space. Each byte of memory is therefore just a definition of the character/graphics symbol required.

Other SAA505X devices may be used when different languages are required. Only 1K byte of memory is needed for either of the Teletext modes, although 20K is reserved for it in mode 135. The MOS uses the spare 19K to speed up inter-filing system file transfers but the user may use this memory if no such transfers are to be done.

The VIDPROC has to be re-programmed to use the SAA5050 RGB outputs.

The 6845 is still used to generate the cursor. As a delay of 2.75 us will occur after a character is read from RAM, before outputting the appropriate RGB signals, the 6845 has to be programmed accordingly. The "start" of screen signal is given a 1.5 byte-time offset, and the SAA5050 has a further 1 byte-time offset to restore the correct cursor/data phase.

The VIDPROC has further adjustment which allows for the cursor to be adjusted to pixel accuracy.

Hardware Scroll:- Scrolling may be achieved in any node by re-programming the 6845 start of screen address to an integral number of video lines further down the memory map than the nominal start of screen.

This of course causes the linear address generator to attempt to display an end of screen which is out of the reserved video area. To overcome this effect, hardware scrolling is provided with a variable address wrap-around.

In effect, when the address generator would otherwise attempt to access out-of-screen RAM, its addresses are modified to point to the gap between the original start of screen and scrolled start of screen. When this is done, only the .end of screen needs to be written over in RAM. (If this is not done, the entire screen appears to "roll-over"). The amount of modification to be used is controlled by two nodes; C0 and Cl as described in figure 6.

Video Output:- Three outputs are provided for displaying video data.

These are:

a) PAL/NTSC encoded, UHF carrier. On channel 36 with 1.5mV into 75 ohm.

b) Composite video. This is a lv peak to peak signal.

c) Digital Red, Green, Blue outputs. These are approximately 75 ohm outputs.

For use with NTSC, the modulator has to be changed from UM1233/E36 to a VHF equivalent. Provision is made for selection of either one of two channels with V.H.F. A Molex type link has to be inserted for this. Link selection is also provided for colour output; either the TV output or the composite video output may have a colour component

Analogue Port:- This 15 way D-type connector provides access to an NEC uPD7002, 4 channel, 10 bit analogue to digital converter. The sampled input is compared to a 1.8V reference derived from three small signal diodes in series.

A tracked link may be cut to deselect this reference. The user may then solder in a two pin precision reference in the holes provided or supply an external reference. Any user supplied reference should have a maximum voltage of 2.5V.

Conversion:- An input voltage on any one of the 4 channels wil be digitised when the A/D control register is so instructed. Conversions are in the range 0 to 1.8v.

The voltage reference is made available at the connector. Provision is made on the board for an additional high stability reference, if required.

A link will have to be made for the additionl reference to be used. Conversions take place in 5mS and the "End of conversion" pulse causes an IRQ to be generated by the system VIA.

Auxiliary Connections:- Two "fire buttons" are provided for with the connections I0, I1. These are connected to the system VIA and cause interrupts (as IRQ) to be generated.

A light pen may be connected to the signal LPSTB. This also causes the system VIA to generate an IRQ (if enabled). It also causes the 6845 CRTC to latch the address of the currently selected video data byte. This may not be the same as the displayed byte, and some software correction may be necessary. Factors such as phosphor characteristics, light pen response and the angle at which the pen is used, may all affect the correction needed.

Serial Ports-Cassette and RS423:- Much circuitry used to provide the RS423 port also generates cassette interface signals. For this reason, these will be described together, with the differences where appropriate.

U.A.R.T.:- The device responsible for providing most of the serial port functions are the 6850 UART. This has all the receive/transmit and data formatting/error checking that is neccessary for both systems.It is fully described in the March 1983 edition of the Hitachi Microcomputer Databook.

SERPROC:- The ACORN proprietary part, the SERPROC is effectively a multiplexer and baud rate generator for the 6850. It also generates the phase-continuous transmission circuitry for use with the cassette interface.

Buffer Components:- The RS423 transmit data and CTS lines are buffered by an AM26L530, or equivalent. This provides a single ended transmission with slew rate limited output.

RS423 receive data and RTS is buffered by a uA9637AC or equivalent. Both buffers are connected with single ended input configurations.

Cassette data output from the SERPROC is buffered by a single, non-inverting operational amplifier with a simple, single pole filter; a.c. coupling capacitor and current limiting output resistor.

2MHz External I/O

Two peripheral devices operate at 2MHz. These are the external second processor connection and the ECONET connection.

ECONET Adapter:- Connection is made to the ECONET by a five way DIN connector mounted on the main circuit board. The interface electronics including the 68B54, line drivers, receivers and chatter disconnnect components are mounted on a separate circuit board. This board has two connectors:-

a) A 5 way connector which has a one-to-one connection with the DIN connector.

b) A 15 way connector provides the CPU data bus together with address , timing reference, chip select and interrupt signals. The main pcb has two further address connections for future expansion.

External Second Processor:- This interface has a buffered data bus via the Wonder Chip. The EXbus on this component provides for good data set up and hold times. Together with a limited degree of line matching, this ensures reliable high speed data transfer with unspecified cable lengths. A maximum cable length of one metre is suggested to prevent noise problems.

The interface operates at 2Mhz. This means that if a 1Mhz bus peripheral is also connected, then the address and data buses on this connector will appear to perform both 1 and 2MHz cycles.

The connections are:-

| | | |
|---|---|---|
| D0 to D7 | Data Bus | CMOS levels |
| A0 to A7 | Address Bus | TTL levels |
| IRQ | Interrupt Request | Open collector TTL levels |
| nTUBE | Parasite chip select | TTL levels |
| Supply | | +5V |
| Ground | | |

# THE MASTER 128 REPAIR GUIDE

**or**

MAT TO DO IF.....

## You get nothing; absolutely nothing:-

1) Is the power switched on (is the keyboard power indicator on)?

2) Listen to the power supply....

Is it 'ticking'? If so try another one. If not, replace anyway as the fuse may have blown. If it still fails, there is a board fault. Locate and repair.

3) Is a monitor connected and switched on?
Is its connecting lead in good order?

4) Try typing 'CTRL G'. If you get a 'beep', try reconnecting the monitor

## Power, but nothing else:-

1) Is power and ground connected to all chips?

2) Are any of the chips hot? Watch for shorts from -5V to the IO controller, causing it to 'latch-up'. If there are any shorts, clear these then replace any affected chips.

*Chips which get abnormally hot during a fault condition but work afterwards should still be replaced. Their long term reliability could still be adversely affected.*

3) Is the system (16MHz) oscillator working?

-WARNING-

If the system clock does not work, the DRAM RAS and CAS lines could be held active LOW. This can make them heat up causing permanent damage. If the oscillator is not working, try to find the cause and repair it as quickly as possible. Do not leave the computer switched on for more than 30 seconds at a time.

4) Are the 1,2,3,4 and 8 MHz signals coming out of the VIDPROC?

5) Is a good 2MHz signal on the CPU clock input?

6) Are all data and address bus lines clear of shorts between themselves, power and ground?
If two or more data bits are faulty within a nibble, suspect the DRAMs connected to that nibble.

7) Are all CPU and PBC data lines connected to where they should be according to the circuit diagram?

8) Are all CPU address lines connected to where they should be, according to the circuit diagram?

9) Is the system ROM plugged in?

10) Are the main DRAMS getting good RAS and CAS signals?
** See the warning above **

11) Is the auxilliary DRAM CAS line high ?
If LOW it will suppress the main DRAMs.

12) Is the DRAM multiplexed address bus correctly switching after RAS with an approximate 20ns hold time?

13) Is the DRAM multiplexed address bus correctly switching after phi2?

<u>You get sort of display with rolling lines and/or diagonal stripes:</u>-

1) Check the 'MA' and 'RA' lines out of the CRTC. Check that these same signals end up at the CRTC MUX. Check that all signal levels are good logic LOWs and HIGHs.

2) Check that VSYNC period is 20mS.
Check that HSYNC period is 64uS.

3) Check that the CSYNC signal works its way to the video output connector that you are using and that its polarity is correct for your monitor.

4) Check all video connections.

<u>You get a cursor stuck at the top left hand corner of the screen:</u>-

1) Check all connections to the keyboard encoder. If they are O.K. then the encoder is probably in serious need of replacement.

2) Do you have a second or co-processor. If so, disconnect it and test it separately, as this could be where the fault is.

<u>You get the 'ACORN MOS' message and 'ACORN ADFS', but nothing else:</u>-

1) Try typing 'CTRL F' and 'BREAK'. If this works then either connect up a disc drive and put an ADFS disc in it or type ' *configure nodir <return>'. Turn the power on and off, it should now be O.K.

2) Is a second or co-processor present? If so, that may be faulty instead.

3) The configuration memory may have been set incorrectly or is faulty. Turn the power off and on, holding down the 'R' key. Then press 'CTRL-F' and 'BREAK'. All previous configuration commands will be reset to zero.

You get the 'BASIC' banner but no '>' prompt:-

1) Comments as above re. second and co-processors.

2) Check IRQ line (pin 4) on CPU. Is this switching up and down (i.e. not stuck high or low)? If so check address lines and chip select of system VIA.

You get the '>' prompt but the keyboard does not respond:-

1) Check the system VIA as above.

2) Check all connections to the keyboard encoder.

3) If all else fails, try a different keyboard. If this works, look for broken leads and tracks on the original one.

4) Check that the IRQ line is not stuck low or high. The memory controller and CMOS clock/RAM both have direct connections to the IRQ line. The latter part has a link which may be used to isolate it from IRQ.

CAUTION : The system VIA generates an interrupt every 100th of a second. If this interrupt is not cleared by the operating system every time it occurs, the IRQ line will appear to be stuck low. This could occur if some other installed software is faulty or if an address or data line to the VIA is faulty.

You can type at the keyboard but not all keys work:-

One of two possible keyboard circuits may be fitted:

a) A 40 pin keyboard encoder on the main circuit board and two 15 way connectors (possibly with an intermediate buffer board) rising to the keyboard matrix.

1) A faulty connection from the encoder to the matrix (or buffer) causing MORE than one key to be affected.

2) A broken track in the middle of a row or column in the keyboard matrix causing MORE than one key to be affected.

3) A broken track at the end of a row or column in the matrix causing ONE key to be affected.

4) A faulty keyswitch causing ONE key to be affected.

N.B. The BEGINNING of a row or column is the end of a pcb trace which is closest to the encoder circuitry. The END of a row or column is the end of a pcb trace which is most distant from the encoder circuitry. The restraints of layout dictate that the beginning or end of a trace is not necessarily the physically closest or furthest.

b) A seventeen way connector rising to a keyboard with the encoder circuitry to the matrix on it.

All of (1) to (4) in the previous paragraph plus :-

1) A faulty connection from the main board to the keyboard encoder circuitry causing MORE than one or the ENTIRE keyboard to be affected.

<u>You get all the keys working, but 'CTRL-BREAK' behaves as ' BREAK':</u>-

('CTRL-BREAK' should invoke the configuration settings.)

1) Check that all power-down components around the CMOS clock/RAM chip are present and have the correct value.

2) Check that pin 13 of the chip is normally HIGH with just occasional excursions LOW.

<u>It only powers up in TERMINAL mode, and *CONFIGURE won't change</u> it: -

Check (1) and (2) above.

1) Check all connections to the clock/RAM chip for open/shorts.

<u>You can use the computer but get random dots or characters on the screen:</u>-

1) Type a short program or piece of text in - about two lines in any screen mode are adequate. Leave it for a few minutes. Has it been corrupted? If so there is a memory system fault. If not enter a longer piece of program or text - enough to fill a screen and repeat the test.

Any fault showing itself will be due to a memory system failure. These are rarely due to the RAM chips themselves - these are usually very reliable chips. Check the following vey carefully:-

a) All connections from the CPU address bus to the DRAM address multiplexers. Then check the voltage levels of these signals at the multiplexer input pins. All signals should have good CMOS levels. A constant 0v or 5v level implies a short to the relevant power rail. Poor logic levels imply shorting to another logic signal.

b) Check that the address at the DRAM inputs is stable for at least 15ns after RAS goes low and changes no later than 50 ns after that edge. This should occur once for every active high period of the system 2MHz clock out of the VIDPROC and once for every active low period.

c) Check that the noise around logic LOW signals is generally less than 500mV. If it is not, then same signals may be shorting or a decoupling capacitor may be missing.

d) Check that the data bus is properly connected between the CPU and the DRAMS.

You can type but get two or more copies around the screen:-

1) Check Test Points (the CRTC scanning outputs) to make sure that the correct addresses are being generated. Any line stuck high or low or shorting to another pin will give strange screen effects. N.B. MA13 is used to switch the address multiplexing circuits between modes 7/135 and any other modes. This line should be static in any given mode.

2) Check that all of the lines from the CRTC to the CRTC Multiplexer actually get there !

3) Check that the lines 'C0' and 'C1' from the 74LS259 to the CRTC Multiplexer are properly connected and change at least once if you switch between modes.

4) Check that the lines from the CRTC multiplexer to the DRAMS are correct with no short or open circuits.

You have a notionally working computer, but have a fault in the:-

Sideways RAM

1) Check all connections to the memory address multiplexers.

2) Check RAS and CAS at the DRAMs.
Are the two links in the correct position for your use ?

Video output which:

Scrolls vertically round the screen...

Does it occur on RGB, UHF and Composite video ?

1) If so, check VSYNC is correct on the CRTC pin 40.

2) Then follow the signal through the exclusive-OR gates where it is combined with HSYNC. If the signal does not make good logic levels at any node, then there is probably a short in that area. N.B. When VSYNC (period 20ms) is EXORed with HSYNC (period 64us), the former will be difficult to

spot within the latter. A way of getting round this is to synchronise the oscilloscope from the VYSNC output of the CRTC and then examine the EXOR gate output.

Does it only occur on one of the video outputs ?

1) Is the CSYNC polarity link correct for your monitor ?

2) If it only occurs on composite video, are all the resistors to the output transistors correct? Do they all have good signals going into them ?

3) If it only occurs on UHF, check the signal as it passes through the resistor network.

4) If it only occurs on RGB, check all the signals going to the back of the connector.

Is correct vertically, but is broken into moving diagonal lines...

Does it occur on RGB, UHF and Composite video ?

1) If so, check HSYNC is correct on the CRTC pin 39.

2) Then follow the signal through the exclusive-OR gates where it is combined with VSYNC. If the signal does not make good logic levels at any node, then there is probably a short in that area. N.B. When HSYNC (period 64us) is EXORed with VSYNC (period 20ms), the former will have the latter superimposed upon it. This will make the former appear to have 'glitches'. This should be ignored in the measurement of HSYNC period.

Does it only occur on one of the video outputs ?

1) Is the CSYNC polarity link correct for your monitor ?

2) If it only occurs on composite video, are all the resistors to the output transistors correct ? Do they all have good signals going into them ?

3) If it only occurs on UHF, check the signal as it passes through the resistor network.

Has no colour on UHF...

1) Is the variable capacitor set to the correct frequency at TP1 ?

2) Check connection to IC40 and resistor summing node through L1 and C81, Q12,C88 and 8140.

3) Check VCC on IC40

4) Try replacing IC 40 as a last resort.

Has only one colour...

On RBG

1) Check the RGB connections out of the VIDPROC

2) Is it just in MODE 7(135)? If so then check RGB connections from SAA5050 to the VIDPROC.

On UHF...

1) Check RGB inputs to IC40. If there are any faults, check the connections from the VIDPROC. If any nodes are stuck at VCC or ground then check for shorts. As a last resort, try changing chips.

2) Check resistors R69,75,77,78,84,85,87,89,90 for the correct values and that they have good signal levels at their IC40 ends.

Has the wrong colours...

Check (1) and (2) above.

Works in all Modes except 7 and 135:-

These Modes work very much differently from the others, using the SAA5050. There are a number of faults which are only exhibited in this mode...

1) There is a cursor which can be moved, but no text.
Check the 6MHz input to the SAA5050. It will have a slightly variable duty cycle, certainly not 50%, but no part of the waveform should be narrower than about 40ns. If so, check all components and signals around the 6MHz generator.

2) The text is at all fragmented - Check as above.

3) Not all colours are present.
Check all connections to the VIDPROC. Are the pull-up resistors present and the correct values?

4) Not all characters can be obtained.
Check all data bus connections the the PBC.

5) Lines of normal size text appear cut in half.
Check VSYNC at the CRTC pin 40.

6) Rounded characters appear unstable.
Check the components and signals around the 6MHz generator.

7) Lines are broken up.
Check all connections to the PBC.

Real time clock which:-

1) Gives strange characters.
Type in the correct time and try again.

2) Does not increment.
Check that the variable capacitor is in the circuit. Check that 32.768 KHz is at the test point. If it does not, check all the values in the oscillator circuit.

3) Are all connections to the system VIA correct ?

4) Are all the components in the chip select/power-down circuit fitted correctly ?

5) Loses a lot of time...
Is the battery flat? Is there at least 2.6V at the clock chip with mains power switched off ?
If not the battery may still be flat, but check the FET and surrounding components first.

Analogue port:-

Gives completely erroneous results on all channels...

1) Are all the connections on the external plug correct?

2) Has it got an incorrect or faulty integration capacitor?

3) Check that the reference voltage is approximately 1.8V and has very little noise on it.

4) Are all the address and data bus connections to it correct?

5) Are the input voltages within the range 0 to 2.5V? If not, the converter will not work correctly.

6) Have any of the terminals in the connector been connected to voltages greater than 5.5V or less than 0.5V? If so the A/D converter is likely to be damaged.

7) Is the chip select from the I0 controller correctly connected ?

8) Does it have a 1MHz timing reference ?

Gives erroneous results on just one channel...

1) The plug and cable connections are the most likely sources of problems.

Point (6) above may also apply.

RS423 port:-

Does not work at all...

1) Are the data format and baud rate settings the sane as the remote computer? CAUTION - These will be set to the configuration values after power on or 'CTRL-BREAK'. Make sure that these are correct as well.

2) Is the cable properly connected? This connector CAN be inserted the wrong way up!

3) Are all the cable connections correct? i.e. no open/short circuits.

4) Are the device select connections to the SERPROC and ACIA from the IO controller correct, with no short circuits to either power supply rail?

5) Is the SERPROC getting a 1.23 MHz timing reference. This could cane from either one of two sources :-

a) A 74LS169 counter b) The chroma chip

Whichever it SHOULD come from is dependent on the build standard of the computer. At any rate, the SERPROC should get this signal from some source. Check that it is the correct frequency.

6) Is the -5V supply correctly connected (and working) to the RS423 transmitter chip?

7) Are either CTS or RTS stuck high or low ?

8) If all else fails, check all remaining connections to the ACIA and SERPROC.

Will only receive data...

1) Does the remote computer use different transmit and receive rates ? If so check that your computer has the equivalent receive and transmit respectively.

2) Check (3), (6) and (7) as above.

3) Check that data going into the line driver comes out of it! The driver could be faulty otherwise.

4) Check that the Tx CLK going into the ACIA is correct.

Will only transmit data...

1) As above.

2) As above.

3) Check that data going into the line receiver comes out of it.

4) Check that the Rx CLK going into the PCIA is correct.

Cassette interface:-

Will not load or save data...

1) Check the cable and data recorder (with another computer if possible).

2) Check that the ACIA and SERPROC have correct (i.e. no open or short circuit) connections on all pins.

3) Check that the back panel connector has no dry joints or short circuits between it and the interface circuitry.

4) Are the connector pins in good condition? If not, the fault could show itself as intermittent operation.

5) Check the 1.23MHz connection to the ACIA.

Will not load data...

Check (1), (3) and (4) above.

1) Check that the ACIA is receiving an Rx CLK.

2) Check the connections between the SERPROC and ACIA.

3) Check that incoming data is appearing at the pin at the back of the connector.

4) Follow the signal path through the high and low pass filters. It should finish up as a 1.2V pk-pk signal at the CASIN input to the SERPROC. If it disappears at any point there is probably a dry joint.

5) The cassette data input has a static protection network on it. Check that all the components in this are fitted and have the correct values. A faulty component could mean that the LM324 has been subsequently damaged.

6) Check (2) and (5) above.

7) As a last resort, change the SERPROC and try again, then try the ACIA. This should not be necessary as both of these components are very reliable.

Will not save data...

Check (1) in the section about complete failure.

1) Check that the ACIA is getting a Tx CLK.

2) Check the connections between the SERPROC and ACIA.

3) Check (3) and (4) in the section about complete failure

4) Check that data is coming out of the CASOUT output from the SERPROC. If not, check all the data and address connections to the SERPROC and ACIA.

4 Follow the signal (if it exists) from the SERPROC to the connector. If it disappears then a dry joint or short to power or ground is likely.

Disc drive interface which:-

Refuses to work at all ...

1) Check that both the signal connector and power connector are securely pushed home.

2) Try another disc drive if possible, to eliminate the chance of a fault in this.

3) Try the disc drive with another computer, if possible.

4) Check that the 1770 and 74LS174 have valid logic levels at their device select inputs and that all data and address bus connections are present, with no open or short circuits.

The drive select light comes on but...

You cannot read a catalogue....

1) Are you using the correct filing system for the disc (i.e. ADFS or DFS)?

2) Is the disc formatted ?

3) Is the disc in the wrong way round ?

4) Is the Read Data input to the 1770 'wiggling' when you attempt to read the disc? If not check the signal cable and if necessary check that data is getting onto it from the disc drive.

5) Are the pull-up resistors on the 1770 disc inputs fitted and correct?

6) Is the 8MHz input to the 1770 correct?

7) Is the 1770 DRQ line normally LOW but going high once every 32us (when then disc interface has been asked to read say, a catalogue)? If not check that this line is not shorted to power or ground and is connected to the I0 Controller.

8) Check that the DRQ transitions appear logically inverted at the NMI pin on the CPU.

9) Check that the 1770 INTRQ output produces a high going pulse at the end of every command issued to the 1770. If the INTRQ line is shorted HIGH it will cause the I0 Controller to hold the CPUs NMI line low, thus masking DRQ transitions.

You can read a catalogue, but the entries are corrupted...

1) (Issue 1 boards only). There should be a small capacitor from the DRQ line to ground. Is this fitted ? Is its value correct ?

2) Are one or two disc drives present ? If two, make sure that only one of them have line termination resistors in.

You can read a catalogue, but cannot get data (or change DIR in ADFS)...

1) Check (1) and (2) above.

You can read data but it is wrong (or you get 'Bad FS map' in ADFS)...

1) Try the disc drive in another computer. If the fault persists, then the disc drive is at fault.

2) (Issue 1 boards only). Check the capacitor from DRQ to ground to ensure that it is connected and the correct value.

3) There may be a fault in the memory system. Check that the address inputs to the Memory Controller are switching with ' good' logic levels. Check that the outputs - the 'AA' and 'AT' lines are switching. A good test here is to repeatedly press ' BREAK' and look at each line in turn.

4) Check that the 'AA' and 'AT' lines are correctly connected to the address multiplexers.

5) Use a memory test program to validate memory. This is rarely necessary as the memory chips are highly reliable.

You can read data correcty but cannot write reliably...

1) Is the disc formatted for DFS but being used with AID'S or vice versa? The built in format is only for use with DFS.

2) Check the disc drive on another computer if possible.

3) Check that data transitions are appearing on the 1770 'WD' and 'WG' pins.

If not check all connections to the 1770 and the 74LS174.

4) Follow the signal path of 'WD' to the connector.

N.B. A disc drive must be connected at this stage as pull-up resistors for the line driver outputs are within the disc drive. The output should be normally HIGH with LOW going transitions.

5) Follow the signal path of 'WG' to the connector.

N.B. A disc drive must be connected at this stage as pull-up resistors for the line driver outputs are within the disc drive. The output should be normally HIGH with IOW going transitions.

You can read and write but can only select one disc drive out of two...

1) Check all connections to the 74LS174.

2) Check that only one drive select output is a logic LOW from the 7438.

Parallel printer port:-

1) Check that the configuration system is set up correctly (i. e. *CONFIGURE PRINT 1). Use the default printer driver to conduct the tests.

2) If the fault only shows up with a custom printer driver, test the software carefully first.

3) Check the printer with another computer if possible.

4) Check the computer with another printer if possible.

5) Check that pin 40 on the User VIA has a pull up to +5V but is not short circuited to +5V.

6) Check that data appearing on Port A of the VIA appears on the outputs of the 74LS244 buffer.

7) Check a strobe pulse appears on pin 39 of the User VIA for every character transmitted. If not, check all address, data and control pins on the User VIA.

8) Check that a strobe pulse is found inverted at pin 11 of the 7438 and true at pin 8 of the 7438.

User port:-

1) Is the software illegal e.g. using 'peek and poke' type commands from a Second or co-processor? If so this is the cause of the problem. It would work on the I/O processor alone but this is not recommended.

2) Is the shift register being used to transfer data on the ' CA' lines? There is a fault in some manufacturers 6522's and for this reason the computer use of this feature of the 6522 is not specified for the computer.

3) Check the software very carefully.

4) Check all address, data and control lines to the User VIA.

5) Have voltages outside the supply range been applied to any of the pins ? If so, the VIA could have been damaged.

N.B. This could arise if a cable is left connected the the User Port and the other end is for instance, left trailing across a carpet.

1MHz bus:-

1) Is there anything in the configuration system that would cause it to be deselected? E.g. configured to power up with the floppy disc drive as the default rather than a hard disc, therefore making the hard disc seem not to work.

2) Ensure that the software has not selected the internal pages &FC and &FD.

3) As with any straightforward parallel data bus, any faults with this have to be found by methodical checking of all connections:-

a) Ensure the remote equipment is not at fault (if possible).

b) Ensure the cables and connectors are in good condition and are correctly assembled i.e. cable clamps are fitted and effective.

c) Ensure that any non-polarised connectors are correctly inserted.

d) Cables longer than 1m should not be used in general.

e) Check that each and every connection is correct as per the circuit diagram.

f) Check that the READY signal from the IO Controller goes to both the CPU and Peripheral Bus Controller (PBC).

g) Check that the FIT connection from the IO controller goes to the PBC.

h) Check that all address connections to the Memory Controller are correct.

i) Check that the two data bus connections to the IO Controller are correct.

'Tube' Connector:-

Check (3 a,b,c,d,e,f,g,h,i) as above

...Sorry !!

Internal Co-processor:-

Not being recognised...

1) Is the configuration status correct ?

2) Are the two connectors correctly mated ?

3) Are two bits of the data bus correctly connected to the IO Controller ?

4) Are all connections to the TWO connectors correct ?

Recognised, but just a cursor in the top left hand corner of the screen...

1) Is the co-processor working ? Try it in another computer.

2) Are the two connectors correctly mated ?

3) Are the boot ROM(s) correctly inserted in the Co-processor ?

Sound output which:-

Will not work with all envelopes...

1) Has your software requested too many channels ?
The envelopes use memory shared with serial data buffer space.

Produces strange sounds whenever a key is pressed..

1) Are all the connections to the sound chip correct ?

2) Try pressing BREAK. If the sound goes away then it may be mains noise affecting the computer. This could happen in places with poor mains supplies.

3) If the worst comes to the worst, try a new 74LS259. This should rarely be needed as the 259 is very reliable.

Will not work at all...

1) Is -5V connected (and working!)?

2) Is the speaker connected.

3) Is there an external speaker (to the sound phono connector at the rear of the machine) which is short circuited or of very low impedance (<= 4 ohms) ?
If so, remove it !

A 'Modem' connector that does not work correctly:-

1) Check the controlling software VERY carefully

3) Check all connections to the connector.

4) Check that a signal arriving at the connector goes through it i.e. no dry joints or faulty connector sockets.

A cartridge port which:-

Causes the sound output to be noisy...

1) Check the cartridge for shorts and general layout.

Will not recognise some cartridges...

1) Is the cartridge for the ELECTRON?

Not all of these are compatible.

2) Are all the links assocciated with the cartridge in the correct possition.

3) Is the cartridge edge connector excessively worn? E.g. gold plating worn through?

4) Are all connections to the edge connectors correct without shorts to each other ?

5) Are any of the edge connector blades bent or worn ?
If so, the connector must be replaced.

**********

BEWARE!!!!!

The Peripheral bus controller is used to buffer the data bus around the system. It also isolates many parts of the system from each other to help improve reliability. It may disguise data bus failures or open circuits. Be sure not to assume that any node is connected to any other unless you have checked it. This particularly applies to the SAA5050 and all 1MHz operating components e.g. the User VIA going down could stop the System VIA.

**********

***** Hints for repair

1) The minimum tools are :-

a) A set of screwdrivers.
b) A reasonably good logic probe.
c) The cicruit diagram.
d) An RGB monitor.
e) Pliers.
f) Cutters
g) A good multimeter.

2) The repair will be quicker with :-

a) 100 MHz oscilloscope.
b) Good quality 'scope probes.
c) Spare peripherals to try.
d) A known good computer to use as a signal model.

3) If you get stuck....ASK.

4) Assume NOTHING (not trite, just good advice!).

5) Do not solder to a 'live' computer.

6) Remove all user ROMs before starting (remember to put them back afterwards!)

7) Use sharp pointed meter probes to push through solder resist. This will make finding short/open circuits more reliable.

8) Always suspect connectors.

10) If you find a recurrent fault (e.g.more than 10 machines), let us at ACORN know so we can included it in this guide if appropriate.

| 8 | 4 | 1 | 1 | Feb '86 |
|---|---|---|---|---|

# 65C102 co-processor user guide

# INTRODUCTION

## What is a co-processor

The job of the co-processor is to run languages such as BASIC, assembly language, word processing, and to run user programs. The TUBE handles the two-way communication between the microcomputer and the co-processor thereby leaving the microcomputer and the co-processor to continue with their respective tasks.

With the co-processor fitted, the job of the microcomputer is to serve as an I/O processor, that is, to handle all the inputs and outputs (keyboard, RS423, text and graphics output to monitors, printer output, disc drives, cassette recorders, local area network and so on).

This co-processor consists of a 65C102 microprocessor system with 64 Kbytes of Random Access Memory (RAM). In addition, it contains an interface between itself and the microcomputer called the TUBE.

From this point on the microcomputer will be referred to as the I/O processor.

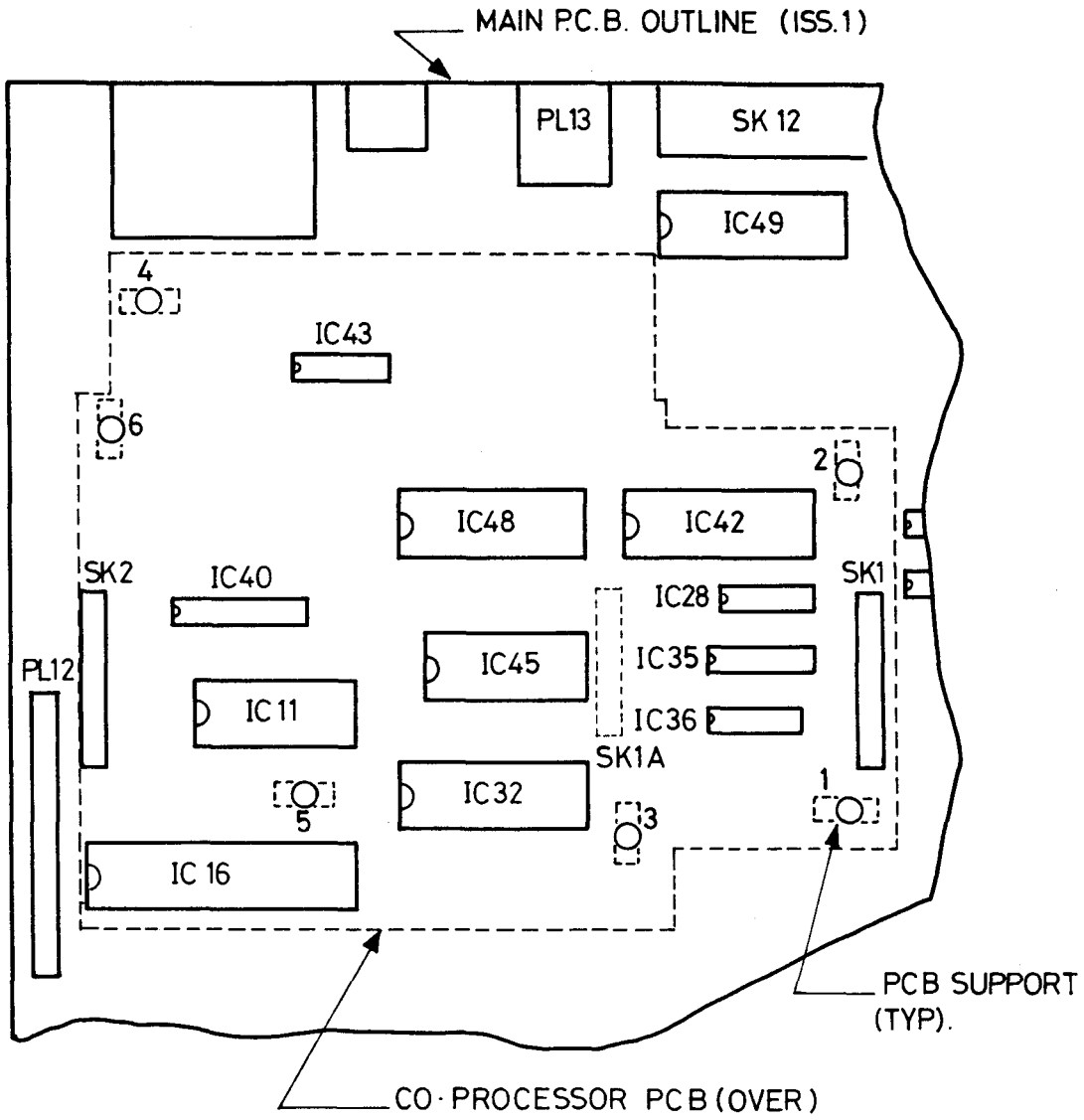
## Fitting a co-processor

Note that any modification or upgrade carried out to the printed circuit board of any Acorn equipment is undertaken at the sole risk of the person carrying out the modification or upgrade. No claim for loss or damage to the equipment caused by the modification or upgrade of the printed circuit board by unqualified personnel shall be accepted by Acorn Computers limited.

WARNING - A number of the components used within ACORN equipment are STATIC SENSITIVE. All usual anti-static precautions must be taken to prevent damage to these devices.

Before attempting this upgrade, please read all the instructions carefully. If you are in doubt about your ability to carry it out, the co-processor and the microcomputer should be taken to your nearest authorised Acorn dealer.

A charge may be levied by the dealer for installing the co-processor; such a charge shall be entirely at the discretion of the dealer concerned.


MAIN P.C.B. OUTLINE (ISS.1)
PL13
SK 12
IC49
4
IC43
6
2
IC48
IC42
SK2
IC40
SK1
IC28
PL12
IC45
IC35
IC 11
IC36
SK1A
IC32
1
5
3
IC 16
PCB SUPPORT
(TYP).
CO·PROCESSOR PCB (OVER)

Dismantling the microcomputer

Before attempting to fit the co-processor to your machine, first ensure that the unit is disconnected from the mains power supply.

The upper half of the case must be removed from the unit to allow access to the main printed circuit board. To do this, turn the computer upside down and place it on a firm, flat surface; locate and remove the four fixing screws that hold the upper half of the case in place. These screws are located on the underside of the unit, two at the rear and two at the front of the machine, and are labelled 'FIX'. Please note that the two fixing screws fitted to the rear fixing positions are longer than the other two.

When the fixing screws have been removed, carefully re-invert the computer whilst holding the two halves of the case together. The upper half of the case may now be removed by lifting it directly upwards from the machine.

Installing the co-processor printed circuit board

Included in the co-processor upgrade kit are a number of plastic printed circuit board support posts. These must be fitted to the main printed circuit board before installing the co-processor board.

The positions at which these posts are to be fitted are shown in figure 1. The posts should be fitted to the positions in numerical order. The first four positions are common to all co-processor options, with positions five and six only in use with certain co-processors. When fitting the P.C.B supports, ensure that the base flange does not interfere with any component on the P.C.B. To fit the support, insert one end into the hole in the P.C.B and press down gently.

When the support is correctly fitted, it will not be possible to withdraw it from the hole in the P.C.B. Care must therefore be taken to ensure the correct positioning of the P.C.B support before pressing it home.

When all the P.C.B supports are installed on the main P.C.B, the co-processor should be placed in position ensuring that:

1. The pins of PL1 on the co-processor are aligned with the corresponding holes in SK1 on the main P.C.B.

2. The pins of PL2 on the co-processor are aligned with the corresponding holes in SK2 on the main P.C.B.

3. The P.C.B supports are aligned with the corresponding holes on the co-processor P.C.B.

When you are satisfied that all the pins and supports are correctly aligned, the co-processor P.C.B may be pressed gently into place. The co-processor is correctly seated when the barbs on the tip of the P.C.B supports have cleared the surface of the co-processor

P.C.B. An audible click should be heard when the barbs spring into place securing the P.C.B.

Take care not to exert too much pressure when pressing home the co-processor P.C.B, this may lead to damage to the various connectors.

When the co-processor P.C.B has been installed, the re-assembly procedure is the reverse of the dismantling procedure.

When the 65C102 co-processor has been installed, the machine should be set up as described in the WELCOME GUIDE. When the machine is switched on a message, similar to the following, should appear on the screen.

ACORN MOS

ACORN ADFS

BASIC

>_

As can be seen from the above message, the 65C102 co-processor does not appear to be present. The reason for the apparent abscence of the co-processor is the CONFIGURATION status of the machine.

To reconfigure the machine to allow for the inclusion of the 65C102 you must use either a *CONFIGURE command, or the control panel included with the WELCOME package. To use the *CONFIGURE command you should enter:

*CONFIGURE TUBE <RETURN>

followed by

*CONFIGURE INTUBE <RETURN>

after entering these two commands you must perform a reset by pressing the BREAK key. This reset is needed to enable the I/O processor to recognise the presence of the co-processor.

After performing the reset, the following message, or something similar, should be displayed:

ACORN TUBE 65C102 CO-PROCESSOR

ACORN ADFS

BASIC

>_

The top line of the display shows that the TUBE and 65C102 co-processor are now recognised by the machine. If the message on your machine does not indicate the presence of the 65C102 co-processor then first use the *STATUS command to determine whether the TUBE is correctly configured, and assuming that the configuration is correct, refer to the ealier part of this section to check that the upgrade has been carried out correctly.

If neither of these courses of action uncover the cause of the problem, the complete machine should be taken to your nearest Acorn registered dealer for testing and, if necessary, repair.

The *CONFIGURE command

The *CONFIGURE command may be used to enable and disable the TUBE communications. It may also be used to select between internal and external TUBE communication. To enable or disable the TUBE communication, *CONFIGURE with TUBE or NOTUBE respectively may be used.

To allow you to add an external co-processor, sometimes referred to as a second processor, you may switch from using the internal TUBE to the external TUBE. This is also carried out using the *CONFIGURE command, this time with INTUBE and EXTUBE respectively.

For further information on the *CONFIGURE command see the REFERENCE MANUAL Part 1.

SYSTEM MEMORY

The following information explains the way in which the memory of both the I/O processor and the co-processor are configured. It is only intended as a general introduction to the memory usage of the two processors. For a more full explanation of the way in which the memory is configured please refer to the REFERENCE MANUAL.

Please note that whilst a general understanding of the systems' memory configuration may be of use, it is by no means essential.

Figure 2 shows the memory map for the I/O processor when it is working with the 65C102 co-processor.

DISTINGUISHING BETWEEN MEMORIES

You will have noticed from the memory map that both the I/O processor and the co-processor are numbered from &0000 to &FFFF. With the co-processor working, the various filing systems must have a way of distinguishing between the two memories in order to SAVE or LOAD programs into the correct place. This is done by defining the co-processor memory as running from &0000 to &FFFF, and the I/O processor memory from &FFFF0000 to &FFFFFFFF.

For example, memory location &C000 resides, by definition, in the co-processor: memory location &FFFFC000 resides in the I/O processor.

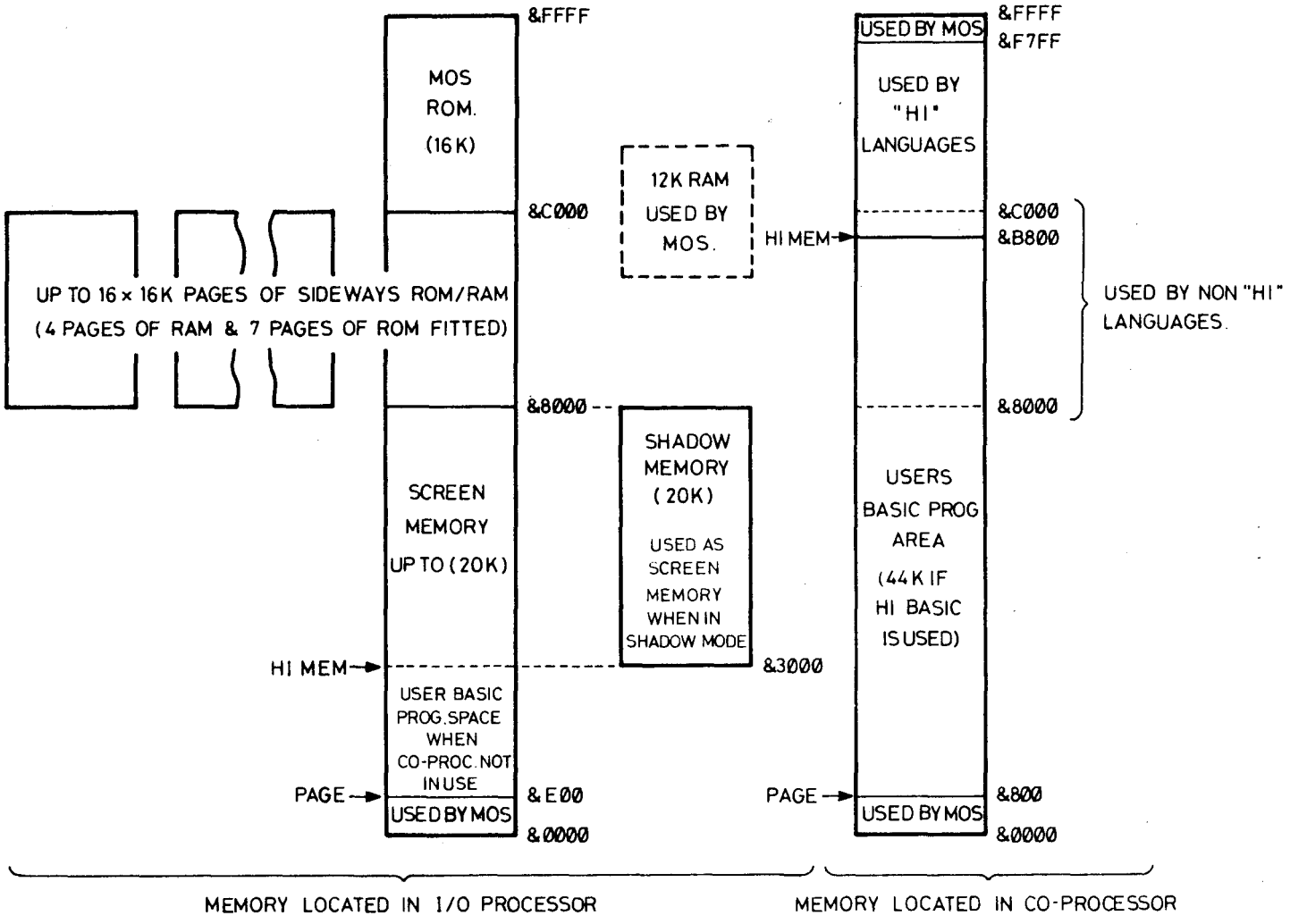
Suppose you run a machine-code program which resides in the co-processor from memory location &6000 to &6500. This program draws a pretty picture on the screen in MODE 1, and you would like to save both the program and the resulting picture onto disc.

To save the program onto disc, you would type:

*SAVE GRAFPRG 6000 6500 <RETURN>

where GRAFPRG is the filename you have chosen. To load and run the

FIG. 2 THE SYSTEM MEMORY MAP



program from disc, you would type:

*RUN GRAFPRG <RETURN>

The program would be loaded back into the co-processor rather than the I/O processor (no leading 'FFFFs' in the load address and end address), and would run.

To save the resulting picture onto disc, you would have to save the screen memory used in MODE 1, this resides in the I/O processor.

MODE 1 screen memory starts at &FFFF3000 and ends at &FFFF7FFF (ie memory locations &3000 to &7FFF in the I/O processor). To save the resulting picture, you would type:

*SAVE PICTURE FFFF3000+5000 <RETURN>

where PICTURE is the filename you have chosen. If you now reload this by typing:

*LOAD PICTURE <RETURN>

the file PICTURE will be loaded into the I/O processor, and as long as you are already in MODE 1, the picture will reappear. (From this you can probably deduce why some programs that directly access the screen will not work with the co-processor.)

Note: It is not possible to save a shadow screen in this way. To save or load a shadow screen you must make use of either the OSWORD calls &5 and &6, or the *FX114 command to 'switch' SHADOW RAM into the main memory map. For further information, please refer to the REFERENCE GUIDE.

You may have noticed that when you execute a *INFO on a disc file, addresses are preceded by either 00 or FF, rather than 0000 and FFFF. For example typing:

*INFO PICTURE <RETURN>

might display

$.PICTURE     FF3000 FF3000 FF4FFF 07A

and typing

*INFO GRAFPRG <RETURN>

might display

$.GRAFPRG     006000 006000 000500 05B

The disc filing system ignores the two most significant bytes of the addressing, the cassette filing system displays the addressing in full.

'extended' addresses. Current versions of BASIC an HI-BASIC make no such distinction. Only the memory in the co-processor can be directly accessed from BASIC. This means that using the ?,! and $ indirection operators to access memory locations in the I/O processor from the co-processor doesn't work, for example:

?&FFFF2000=&55 <RETURN>

will put the value &55 into memory location &2000 in the co-processor and not into the location &2000 in the I/O processor as specified by the leading FFFFs.

The same applies to saving and loading BASIC programs. If you save a BASIC program to disc or cassette from the microcomputer, executing a *INFO will display addresses with leading FFs. Saving a BASIC program from the co-processor and executing a *INFO will display addresses with leading 00s. However, BASIC will always load either program into whichever processor is currently running BASIC.

It is possible to read and write to memory locations in the I/O processor memory, this is done using OSWORD calls 5 and 6. OSWORD calls are dealt with in the REFERENCE MANUAL Part 1. A more advanced description of TUBE communication techniques is contained within the ADVANCED REFERENCE MANUAL.

## The 65C102 co-processor support disc

The disc supplied with the 65C102 contains 3 pieces of software, these are:

HiBASIC

HiEDIT

Printer buffer utility

## Hi languages

HiBASIC and HiEDIT are the same languages BASIC and EDIT that are already resident in your machine. They only differ from the inherent versions in the position that they expect to occupy within the memory map.

If we consider the memory map of the microcomputer without a co-processor attached (fig.2), we can see that BASIC normally resides between &8000 and &BFFF. If BASIC were allowed to do this within the co-processor, it would substantially reduce the amount of RAM available to the users programs. HiBASIC is supplied to overcome this situation, it does so by locating itself between addresses &B800 and &F7FF in the co-processor thereby allowing the user to maximise the RAM available. HiEDIT, in this respect, acts in exactly the same way as HiBASIC.

To use either HiBASIC or HiEDIT, insert the 65C102 support disc into the disc drive and enter:

*HiBASIC <RETURN>

(or)

*Hi EDIT <RETURN>

depending on the language you wish to use.

Printer buffer utility

On the 65C102 Support Disc, along with HiBASIC and HiEDIT, you will find a file called BUFFER.

A buffer is an area of RAM that is used as a 'holding area' for data that is in transit between the microcomputer and an external device. The RAM may be part of either the microcomputer, or the external device, and is part of the communications pathway through which the two devices communicate.

The size of a particular buffer can make a considerable difference to the speed and efficiency of a given data transfer. In the case of the microcomputers' printer buffer, there is a 256 byte area of RAM allocated to this purpose. This means that as soon as the microcomputer has transmitted 256 bytes of data more than the printer has accepted, the buffer will become full, and the microcomputer will be forced to wait until more space becomes available in the printer buffer.

The length of time the computer, and therefore the operator, spends waiting is dependant upon three things:

a) The speed at which the printer can print
b) The size of the receive buffer contained within the printer
c) The size of the transmit buffer in the microcomputer

Both a) and b) are determined by the design of the printer and are not easily changed; the size of the default printer buffer in the microcomputer is also fixed. It is however possible to re-allocate the area of the microcomputers' memory to be used as a printer buffer; this is the function of the printer buffer utility.

This utility provides you with approximately 24 Kbytes of buffer in the I/O processor for use with your currently selected printer. This dramatic increase in buffer size means that the the computer will not have to wait for the printer unless the data to be printed exceeds 24 Kbytes. In the instance of a text file, this may be considered to be roughly equivalent to 24 A4 pages of text, sufficient to hold the entire textual content of this manual with room to spare!

This buffer uses RAM in the I/O processor between &4000 and &8000 and should not be used where your own application makes use of this area of I/O memory. Since the area of memory used by the printer buffer utility is the same as that available to the user when a co-processor is not in use; this utility may only be used in conjunction with a co-processor.

To make use of the printer buffer utility, you should enter:

*BUFFER

It is important to realise that, whilst you are able to continue using a word processor, or other language resident in the co-processor, it is not possible to make use of the main RAM in the I/O processor whilst the printer buffer is in use. This will preclude the use of a number of other utilities such as AFORM and the Q parameter available with the sideways RAM utilities. Also, you should realise that a 20 Kbyte text file can take as much as 15 minutes to print on a slower printer. The microcomputer should be neither reset or switched off whilst the printer is still printing.

For further information on the use of printers, please refer to the WELCOME GUIDE that accompanied the microcomputer.

# Fitting an ECONET module

**Note that any modification or upgrade carried out to the printed circuit board of any Acorn equipment is undertaken at the sole risk of the person carrying out the modification or upgrade. No claim for loss or damage to the equipment caused by the modification or upgrade of the printed circuit board by unqualified personnel shall be accepted by Acorn Computers limited.**

**WARNING - A number of the components used within ACORN equipment are STATIC SENSITIVE. All usual anti-static precautions must be taken to prevent damage to these devices.**

**Before attempting this upgrade, please read all the instructions carefully. If you are in doubt about your ability to carry it out, the ECONET module and the microcomputer should be taken to your nearest authorised Acorn dealer.**

**A charge may be levied by the dealer for installing the ECONET module; such a charge shall be entirely at the discretion of the dealer concerned.**

## Dismantling the microcomputer

Before attempting to fit the ECONET module to your machine, first ensure that the unit is disconnected from the mains power supply.

The upper half of the case must be removed from the unit to allow access to the main printed circuit board. To do this, turn the computer upside down and place it on a firm, flat surface; locate and remove the four fixing screws that hold the upper half of the case in place. These screws are located on the underside of the unit, two at the rear and two at the front of the machine, and are labelled 'FIX'. Please note that the two fixing screws fitted to the rear fixing positions are longer than the other two.

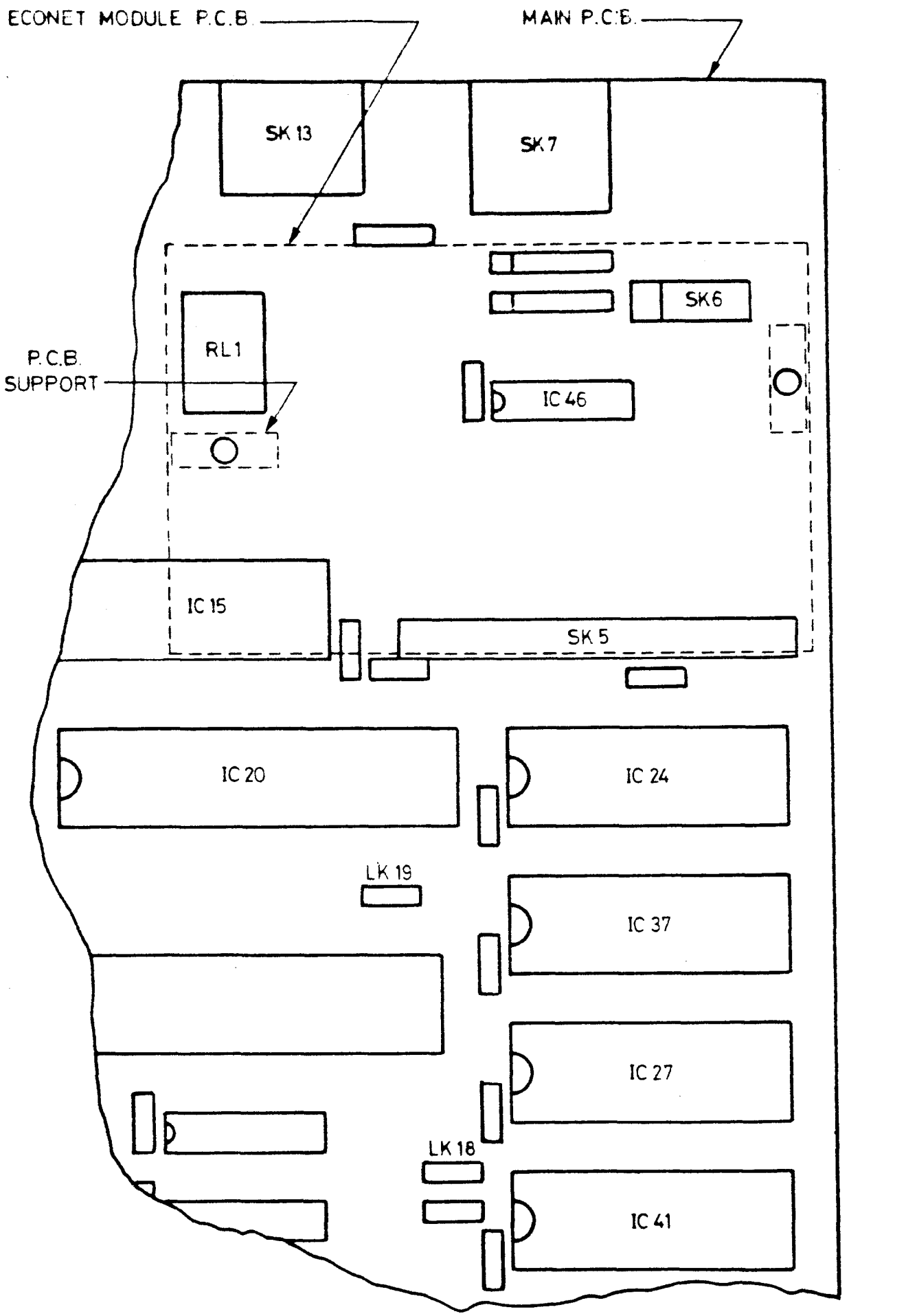
When the fixing screws have been removed, carefully re-invert the computer whilst holding the two halves of the case together. The upper half of the case may now be removed by lifting it directly upwards from the machine.

## Machine orientation

Within this fitting instruction, the points of the compass are used to indicate the way in which things are orientated. With the machine positioned such that the keyboard is nearest you and uppermost, the nearest edge is designated to be SOUTH, the rear NORTH and right and left are designated EAST and WEST respectively.

The ECONET module will be installed in the NORTH-EAST corner of the main printed circuit board

| 8 | 5 | 1 | 2 | Feb '86 |
|---|---|---|---|---|


ECONET MODULE P.C.B.
MAIN P.C.B.
SK 13
SK 7
SK6
RL1
P.C.B.
SUPPORT
IC 46
IC 15
SK 5
IC 20
IC 24
LK 19
IC 37
IC 27
LK 18
IC 41

**Installing the ECONET module printed circuit board**

Included in the ECONET module upgrade kit are two plastic printed circuit board support posts. These must be fitted to the main printed circuit board before installing the ECONET module.

The positions at which these posts are to be fitted are shown in figure 1. When fitting the P.C.B supports, ensure that the base flange does not interfere with any component on the P.C.B. To fit the support, insert one end into the hole in the P.C.B and press down gently.

When the support is correctly fitted, it will not be possible to withdraw it from the hole in the P.C.B. Care must therefore be taken to ensure the correct positioning of the P.C.B support before pressing it home.

When the P.C.B supports are installed on the main P.C.B, the ECONET module should be placed in position ensuring that:

1. The pins of PL1 on the ECONET module are aligned with the corresponding holes in SK5 on the main P.C.B. The two WEST most holes of SK5, labelled 'a' and 'b', are not used.

2. The pins of PL2 on the ECONET module are aligned with the corresponding holes in SK6 on the main P.C.B.

3. The P.C.B supports are aligned with the corresponding holes on the ECONET module P.C.B.

When you are satisfied that all the pins and supports are correctly aligned, the ECONET module P.C.B may be pressed gently into place. The ECONET module is correctly seated when the barbs on the tips of the P.C.B supports have cleared the surface of the ECONET module P.C.B. An audible click should be heard when the barbs spring into place securing the P.C.B.

Take care not to exert too much pressure when pressing home the ECONET module P.C.B, this may lead to damage of the various connectors.

Installing the ANFS

Having fitted the ECONET module, it is necessary to fit the Advanced Network Filing System (ANFS) ROM.

The ANFS ROM must be inserted into one of three sockets, IC27,37 or 41. It is recommended that socket IC27 should be used where possible. If it is not possible to use socket IC27 then one of the other two sockets may be used, but it will be necessary to change the position of a link on the main P.C.B (see NOTE 1).

To insert the ANFS ROM, hold the ends of the IC between thumb and forefinger, and line up all the pins over the destination socket.

The pin 1 end of the IC (see NOTE 2) should face to the WEST. If you are unsure of which way round the IC should be installed, refer to the other ICs on the main PCB which all face WEST.

Apply firm pressure to the IC, but do not force it. When the chip is in place it may appear to be slightly raised. Check that all the pins have entered the socket and that none are bent either outwards or under the body of the IC.

When the ECONET module P.C.B and the ANFS ROM have been installed, the re-assembly procedure is the reverse of the dismantling procedure.

**Setting the station number**

Before attempting to add a machine to an existing ECONET, the station number must be set. The network manager should be asked to carry out this operation.

NOTE 1: Sockets IC37 and 41 share the same address space as four sideways RAM pages. The position of links LK18 and LK19 determine whether the address space is claimed by ROM or sideways RAM.

These two links are located close to the WEST side of ICs37 and 41 ( see fig 1.), LK18 is used with IC41 and LK19 is used with IC37. These links consist of a three pin plug with a connector which may be push fitted onto two pins of the plug to make a connection. There are two possible positions for this connector:

EAST - the connector joins the central pin to the right hand pin ( enables sideways ROM)
or

WEST - the connector joins the central pin to the left hand pin ( enables sideways RAM)

The use of one of the sockets with a ROM will preclude the use of 32K (two 16K pages) of sideways RAM. If both IC37 and IC41 are used in conjunction with sideways ROMs, all four of the 16K sideways RAM pages will be unavailable.

If IC27 is already occupied and you need all four pages of sideways RAM, you will need to fit the ANFS ROM into an EPROM cartridge which can then be plugged into one of the cartridge sockets.

Further information about the use of sideways RAM/ROM may be obtained from part 2 of the REFERENCE MANUAL.

NOTE 2: Pin one is indicated in one of two ways. Either a small dot or dimple is placed directly above pin one, or a horeshoe shaped indentation is cut into the pin one end of the IC with pin one always being to the left of the indentation. In some instances both of these indicators will be present.

# Advanced Additional information relating to Master Repair Guide

Problem: Loss of configuration

Solution:

1) Replace C11 by 100uF capacitor (0610,100)
2) Replace D8 by IN4001 (0794,001)
3) Fit 1K8 resistor (0502,182) between the base and emitter of Q3 on the solder side of the board.

Problem: Break up in Mode 7

Solution:

Add a 100pF capacitor to C30; this should only be necessary for machines bought before 3.2.86.

Problem: Unit crashes after a period of time ie operation becomes unreliable. Test by heating 74S04 (IC 43) to approximately 55 degree C - this usually occurs on National semi conductor chips).

Solution:

Change capacitors C85 & C86 from 100pF to 10nF (629,010)

Problem: Unable to obtain colour on the Composite Video Output.

Solution:

Connect a 470pF capacitor between the East leg of R137 & the East leg of 8153 which are located directly east of the modulator. Connections should be made on the component side of the board with the leads of the 470pF capacitor being soldered directly to the leads of the two resistors.