Chapter 10 Podules and backplane

10.1 Introduction

A podule is the general expansion mechanism for ARM based computer systems. This chapter defines the physical and electrical standards of the podule system and the operating system independent parts of the software interface. It is assumed that the reader is familiar with the basic concepts of the ARM based computer systems. Refer to the ARM, MEMC and IOC data sheets. (See the Bibliography in Appendix H.)

In general, podules are PCBs to the Eurocard standard which plug into a backplane inside the machine. The backplane in turn plugs into the main computer PCB. Each podule has an integral back panel which gives provision for connectors to the outside world.

Podules normally have a 64 way DIN 41612ac connector, with the a and c rows loaded. In addition, a coprocessor podule requires the b row to be loaded. The interface for a coprocessor podule is a 96 way DIN 41612abc connector.

Physical dimensions

Podules are constructed to the Eurocard specification and are mounted horizontally. Podules may be either single or double width (ie height in the normal Eurocard specification). Podules are 5HP (1 inch) high. A double width podule, when viewed from above with the external connectors towards you, should have its podule connector fitted in the left-hand position.

Fitting a podule

Before fitting or removing a podule, ensure that the Acorn Technical Publishing System is switched off and disconnected from the mains supply.

Fitting

1. Remove the three M3 bolts at the rear of the Acorn Technical Publishing System that fasten the base unit to the cover. These are located at either side and in the top centre.

2. Disconnect any cables connected to the unit that may hinder removal of the base.

3. Slide out the base unit from the cover until the podule expansion area is fully exposed. It is recommended that the base unit is not withdrawn further than necessary.

4. Slide in the podule from the rear, guiding it carefully so that it mates with the appropriate backplane expansion socket

5. Fasten the podule back panel to the rear of the Acorn Technical Publishing System using the M2:5 bolts supplied with the podule.

6. Slide the base unit back into its cover, and refasten the three M3 screws.

Removal

It will not usually be necessary to withdraw the Acorn Technical Publishing System base unit from its cover.

Single podule
- Undo the M2.5 screws that hold the ends of the podule back panel to the rear face of the base. Withdraw the podule.

Double podule
- Undo the two M2.5 screws that hold the ends of the podule back panel to the rear face of the base. Withdraw the podule.

Types of podule

At present there are three basic types of podule:

- simple podules
- MEMC podules
- coprocessor podules.

Simple podules
These podules occupy the IOC address space allocated to podules, and are accessed via one of the four IOC cycle types. Most podules will be of this type.

MEMC podules
These podules attach directly to the MEMC IORQ*/IOGT* interface, and occupy the non-IOC address space. Each of these podules can occupy up to 8 kbytes of address space. The cycle timing of these podules must be determined by a state machine on the podule. A podule of this category also appears *as a* simple podule, with the simple podule mapping used for control, and the MEMC podule mapping used for data transfer. Care must be taken in this case as the simple podule timing is derived from CLK8 and the MEMC podule timing is derived from REF8M and the phase relationship between the two clocks cannot be guaranteed.

Coprocessor podules
Coprocessor podules share the same interface as other podules, but they are not mapped into the I/O space as are other podules. In addition to the normal podule signals, coprocessors require access to the main system data bus, and extra control signals. These are provided by a special coprocessor podule connector, which has 96 pins. When a coprocessor is not required, this connector may be used as a normal podule slot. Note that in this context the term 'coprocessor' refers to a dedicated hardware processor, and not an additional general purpose microprocessor system. This class of podule is only briefly referred to in this document.

10.2 Podules In the I/O system

This section outlines the I/O system implemented on present ARM based computer systems. It is important to realise that future systems may have a different implementation of the I/O system, and in particular the addresses (and number) of podule locations may change. For this reason, and to ensure that any device may be plugged into any slot, all driver codes for podules must be relocatable. References to the direct podule addresses should never be used. It is up to the machine operating system, in conjunction with the podule ID, to determine the address at which a podule should be accessed. To this extent, the sections *System architecture, System memory map* and *I/O space memory map* below are for background information only.

System architecture

The I/O system (which includes podule devices) consists of a 16 bit data bus (BD[0:15]), a buffered address bus (LA[2:21]) and various control and timing signals. The I/O data bus is independent from the main 32 bit system data bus, being separated from it by bidirectional latches and buffers (see the figure below). In this way the I/O data bus can run at much slower speeds than the main system bus to cater for slower peripheral devices. The latches between the two buses, and hence the I/O bus timing, are controlled by the I/O controller, IOC. The IOC caters for four different cycle speeds (slow, medium, fast and synchronous) and the programmer can choose the most suitable one for each device.

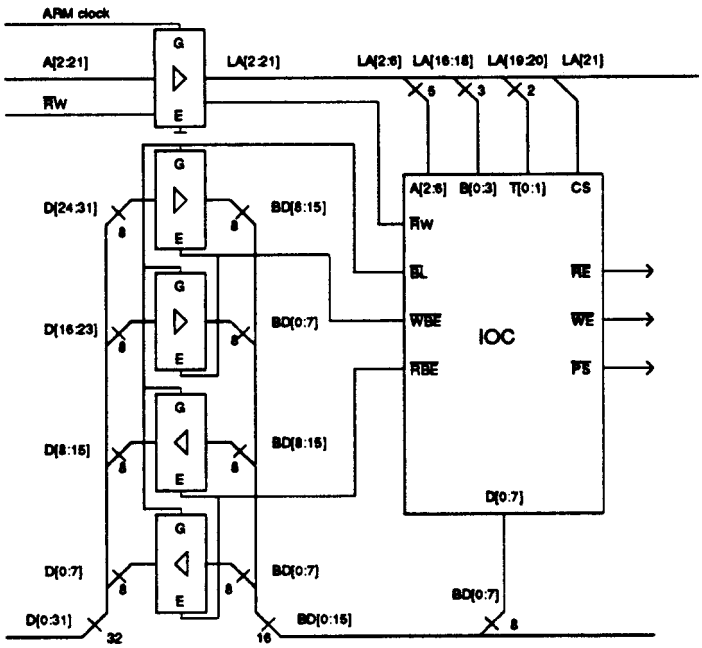


Figure 10.1 : System architecture

A typical I/O system with podules fitted is shown in the figure below. The simple podules are controlled by IOC, and the MEMC podules share the I/O controller interface with IOC. For clarity, the data and address buses are omitted from this diagram.

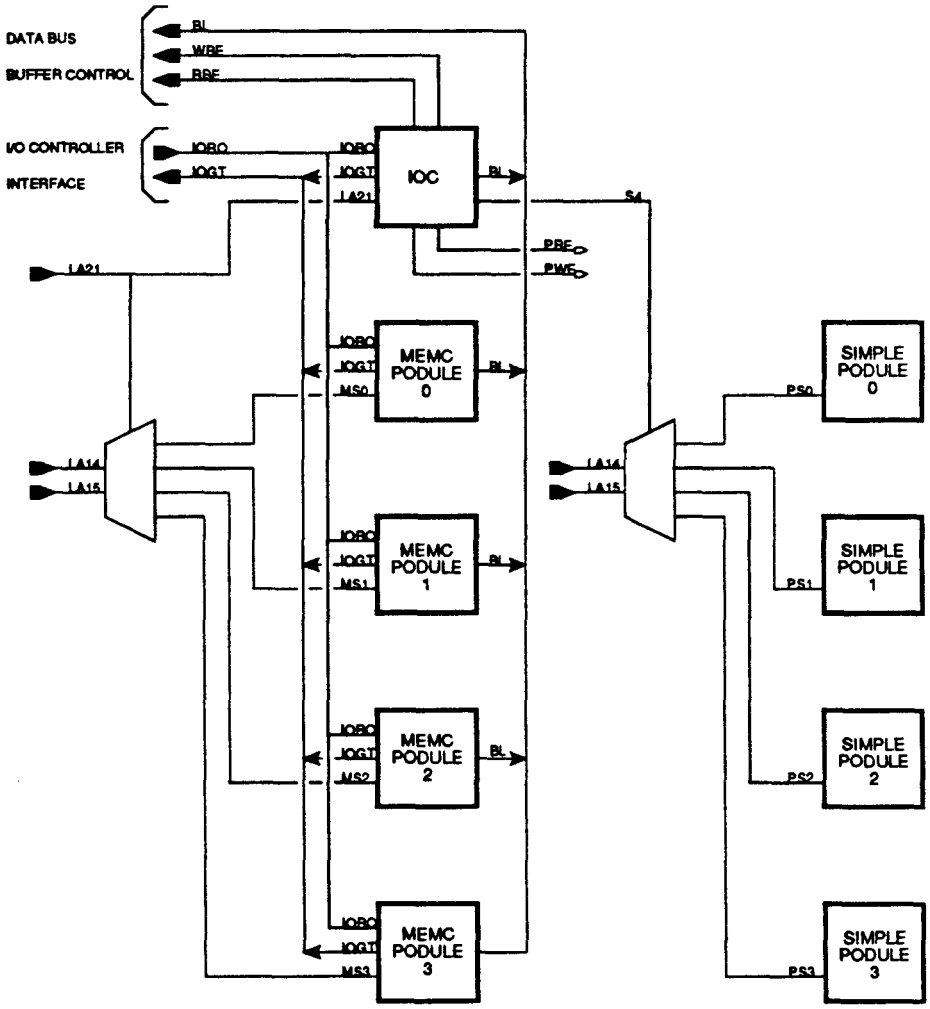


Figure 10.2: Typical I/O system with podules fitted

Non-IOC devices

The IOC is mapped to control devices in the upper half of the I/0 space. The lower half of the I/O space may be used by other devices which are not mapped through, or timed by the IOC. Such devices (normally MEMC podules) share the same handshaking control lines to the MEMC as does the IOC (the I/O controller interface). The advantage of devices in this class are that they are not tied to one of the four possible IOC cycle types.

System memory map

The system memory map is defined by the MEMC, and is shown in Figure 10.3 below. Note that all system components, including I/O devices, are memory mapped.

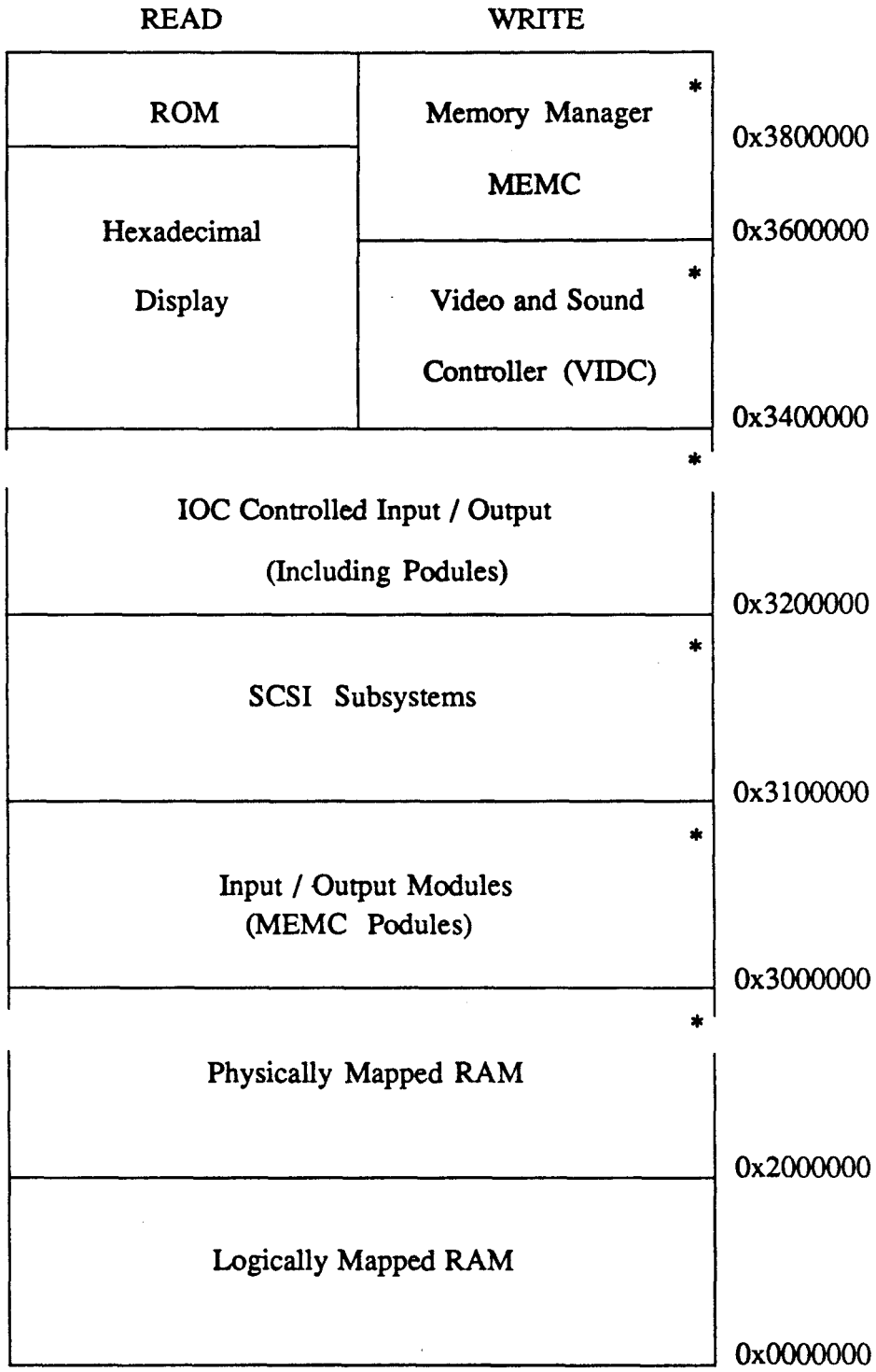


Figure 10.3 : System memory map

The areas marked '*' are accessible only to processes running in the supervisor mode.

I/O space memory map

The I/O space is split into two, with the upper half being controlled by IOC, and the lower half allocated to non-IOC mapped devices (normally MEMC podules). Only the lower part of the non-IOC mapped device space may be used at present. The IOC-controlled space has allocation for simple podules and external podules. The MEMC podule and simple podule spaces are divided into four equal parts, with one part being allocated to each physical podule slot (see the figure below). Present systems may have up to four podule slots, designated slots 0 to 3. In this way, each physical slot is identical, but each appears separately in the address space. The way in which the existence of a podule is identified is explained in the section *Podule identity* below.

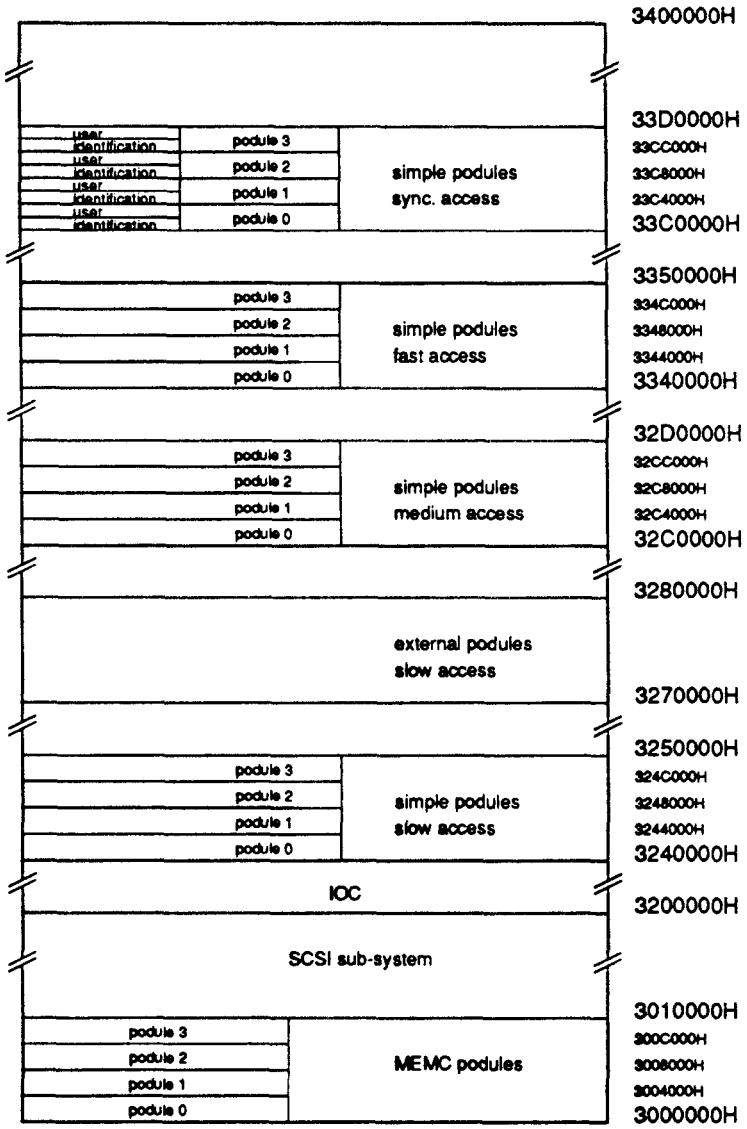


Figure 10.4 : I/O space memory map

Podule access speed

Simple podules
The simple podules are mapped through the IOC, and may be accessed at one of four different cycle speeds as determined by the address at which they are selected. The four cycle types are designated slow, medium, fast and synchronous. Their timings are detailed in the section *Simple podules* below. Their address mapping is shown in Figure 10.4 above.

MEMC podules
The cycle timing of MEMC podules must be driven by the podule itself. A simple state machine clocked by the 8 MHz reference signal is usually required to control these cycles. Refer to the section *MEMC podules* below.

Podule size

The podule data bus is 16 bits wide, enabling byte or half-word accesses. MEMC podules may address 8 kbytes of data each. Simple podules also occupy an 8 kbyte space, but some of this space *is* allocated to podule identification, the exact amount being chosen by the designer. Refer to the section *Podule identity* below.

Data bus mapping

The I/O data bus is 16 bits wide. Bytewide accesses may of course be used for eight bit peripherals. The I/O data bus (BD[0:15]) connects to the main system data bus (D[0:31]) via a set of bidirectional data latches.

The mapping of the BD[0:15] bus onto the D[0:31] bus is as follows:

- During a WRITE (ie ARM to peripheral) BD[0:15] is mapped to D[16:31]
- During a READ (ie peripheral to ARM) BD[0:15] is mapped to D[0:15]

Byte accesses
To access bytewide podules, byte instructions should be used. When a byte store instruction is executed, the CPU will place the written byte on all four bytes of the word, and will therefore correctly place the desired value on the lowest byte of the I/O bus. A byte or word load may be used to read a bytewide podule into the lowest byte of an ARM register. For example:

```
...
...
LoadByte
LDRB Rdata, [Raddress]
...
...
StoreByte
STRB Rdata, [Raddress]
...
...
```

Half-word accesses
To access a 16 bit wide podule, word instructions should be used. When storing, the half-word must be placed on the upper 16 bits, D[16:31]. To maintain upwards compatibility with future machines, half-word stores should replicate the written data on the lower half-word, D[0:15]. When reading, the upper 16 bits are undefined. For example:

```
...
...
LoadHalfWord
    LDR Rdata, [Raddress]
    MOV Rdata, Rdata, ASL#16
    MOV Rdata, Rdata, ASR#16
...
...
StoreHalfWord
    MOV Rdata, Rdata, ASL#16
    ORR Rdata, Rdata, Rdata, ASR#16
    STR  Rdata, [Raddress]
...
...
```

Word accesses
Word-wide podules are not currently supported by the podule bus.

Podule Interrupt handling

There are two interrupt Enes on the podule bus, PIRQ* and PFIQ*. Both lines are vectored through the IOC and generate ARM IRQ* and FIQ* signals respectively. PIRQ* is the normal interrupt request line, and appears as bit 5 in the IOC IRQ status B register (address 3200020H). PFIQ* is the fast interrupt request line, and appears as bit 6 in the IOC FIQ status register (address 3200030H). For further details on interrupt handling refer to the IOC data sheet. Note that future systems may have a different implementation of the I/O system, and in particular the addresses (and number) of podule locations may change.

A podule generating an IRQ* interrupt must drive the PIRQ* line low. Both interrupt lines have a resistive pullup of 1k2 Q. In order that the ARM can determine which podule *is* generating the interrupt, a podule which is driving the PIRQ* line low must also set its IRQ status bit high.

A podule generating a FIQ* interrupt must drive the PFIQ*line low. In order that the ARM can determine which podule is generating the interrupt, a podule which is driving the PFIQ* line low must also set its FIQ status bit high.

Podule Interrupt mask register

As an extension to the standard Archimedes, the Acorn Technical Publishing System backplane printed circuit board contains a podule interrupt mask register .

This register allows individual podule IRQ interrupts to be masked off, and provides a means of implementing an interrupt priority level scheme for podules.

Writing a '0' to a bit in the podule interrupt mask register disables interrupts from the corresponding slot on the backplane.

Writing a '1' to a bit in the podule interrupt mask register enables interrupts from the corresponding slot on the backplane.

The mechanism for identifying which slot is generating the interrupt is described in the section *Podule identity* below.

The mechanism for clearing the interrupt from a particular slot will depend on the device installed in that slot.

This register is external to IOC and is located at the address in Table 5.2 in Chapter 5, *The input/output system*.

The bit positions correspond to the slot number as shown in the table below.

BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
RSVD	RSVD	RSVD	RSVD	slt 3	slt 2	slt 1	slt 0

RSVD = Reserved, Write 0, disabled

Table 10.1 : Podule interrupt mask register

Podule Interrupt status register

As an extension to the standard Archimedes, the Acorn Technical Publishing System backplane contains a podule interrupt status register.

This register allows the processor to identify which podule is generating the interrupt without scanning the IRQ flag on each podule. The status register is read only.

A logic one read in a bit position indicates that the slot is enabled and interrupting.

Podule Identification

It is important that the system is able to identify what podules (if any) are present, and where they are.

This is done by reading the podule identification (PI) byte, or bytes, from the podule identification field. Refer to the section *Podule identity* below.

10:3 The podule bus connectors and loading

The podule bus is an extension of the I/O data and address buses, and carries the necessary control signals.

Simple podule and MEMC podule Interface

The podule interface consists of a 64 way DIN 41612ac connector. It is defined as follows:

pin	a	c	
1	0V	0V	ground
2	LA[15]	-5V	supply
3	LA[14]	0V	ground
4	LA[13]	0V	ground
5	LA[12]	reserved	
6	LA[11]	MS*	MEMC podule select
7	LA[10]	*reserved*	
8	LA[9]	*reserved*	
9	LA[8]	*reserved*	
10	LA[7]	*reserved*	
11	LA[6]	*reserved*	
12	LA[5]	RST*	reset (see note)
13	LA[4]	PR/W*	read / not write
14	LA[3]	PWE*	write strobe
15	LA[2]	PRE*	read strobe
16	BD[15]	PIRQ*	normal interrupt
17	BD[14]	PFIQ*	fast interrupt
18	BD[13]	*reserved*	
19	BD[12]	C1	I^2C serial bus clock
20	BD[11]	C0	I^2C serial bus data
21	BD[10]	EXTPS*	external podule select
22	BD[9]	PS*	simple podule select
23	BD[8]	IOGT*	MEMC podule handshake
24	BD[7]	IORQ*	MEMC podule request
25	BD[6]	BL*	I/O data latch control
26	BD[5]	0V	supply
27	BD[4]	CLK2	2 MHz synchronous clock
28	BD[3]	CLK8	8 MHz synchronous clock
29	BD[2]	REF8M	8 MHz reference clock
30	BD[1]	+5V	supply
31	BD[0]	*reserved*	
32	+5V	+12V	supply

Table 10.2: Simple podule and MEMC podule interface

The reserved pins must be left unused as in some machines these pins carry coprocessor signals.

Note: The RST* signal is the system reset signal, driven by IOC on power-up or by the keyboard reset switch (when link is connected). It is an open-collector signal, and podules *may* drive it also if this is desirable. The pulse width should be at least 50 ms.

Coprocessor podule Interface

The coprocessor podule interface is a 96 way DIN 41612abc connector. It is the same as a normal podule connector except that the b row is loaded with the main system data bus, and most of the reserved pins are allocated.

pin	a	b	c	
1	0V	D[0]	0V	
2	LA[15]	D[1]	-5V	
3	LA[14]	D[2]	0V	
4	LA[13]	D[3]	0V	
5	LA[12]	D[4]	SPVMD	supervisor mode
6	LA[11]	D[5]	MS*	
7	LA[10]	D[6]	CPA	coprocessor absent
8	LA[9]	D[7]	CPB	coprocessor busy
9	LA[8]	D[8]	CPI*	coprocessor instruction
10	LA[7]	D[9]	OPC	op-code fetch
11	LA[6]	D[10]	PHI2	ARM phase 2 clock
12	LA[5]	D[11]	RST*	
13	LA[4]	D[12]	PR/W*	
14	LA[3]	D[13]	PWE*	
15	LA[2]	D[14]	PRE*	
16	BD[15]	D[15]	PIRQ*	
17	BD[14]	D[16]	PFIQ*	
18	BD[13]	D[17]	*reserved*	
19	BD[12]	D[18]	C1	
20	BD[11]	D[19]	C0	
21	BD[10]	D[20]	EXTPS*	
22	BD[9]	D[21]	PS*	
23	BD[8]	D[22]	IOGT*	
24	BD[7]	D[23]	IORQ*	
25	BD[6]	D[24]	BL*	
26	BD[5]	D[25]	0V	
27	BD[4]	D[26]	CLK2	
28	BD[3]	D[27]	CLK8	
29	BD[2]	D[28]	REF8M	
30	BD[1]	D[29]	+5V	
31	BD[0]	D[30]	DBE	ARM data bus enable
32	+5V	D[31]	+12V	

Table 10.3 : Coprocessor podule interface

Main PCB connector

The connector fitted to the main PCB is broadly similar to the coprocessor interface without the power pins and without the individual podule select lines. The backplane receives 0 V, +5 V and +12 V directly from the power supply.

The backplane supports four podules, one of which can be a coprocessor, and generates the individual podule select lines (PS* and MS*) from the master simple podule select (S4*) and MEMC podule select (MODULE*) lines. It uses LA[14] and LA[15] to decode the four podules.

The coprocessor podule interface is on podule slot 2. The signals which are dedicated to coprocessor functions (and which are reserved on the other podule slots) are only tracked to podule slot 2. This includes the whole of the b row of the connector (D[0:31]).

The connector on the main PCB is as follows:

pin	a	b	c	
1	0V	D[0]	0V	
2	LA[15]	D[1]	-5V	
3	LA[14]	D[2]	0V	
4	LA[13]	D[3]	0V	
5	LA[12]	D[4]	SPVMD	
6	LA[11]	D[5]	MODULE*	
7	LA[10]	D[6]	CPA	
8	LA[9]	D[7]	CPB	
9	LA[8]	D[8]	CPI	
10	LA[7]	D[9]	OPC	
11	LA[6]	D[10]	PHI2	
12	LA[5]	D[11]	RST*	
13	LA[4]	D[12]	PR/W*	
14	LA[3]	D[13]	PWE*	
15	LA[2]	D[14]	PRE*	
16	BD[15]	D[15]	PIRQ*	
17	BD[14]	D[161	PFIQ*	
18	BD[13]	D[17]	S6*	IRQ mask/status select
19	BD[12]	D[18]	CI	
20	BD[11]	D[19]	C0	
21	BD[10]	D[20]	EXTPS*	
22	BD[9]	D[21]	S4	master podule select
23	BD[8]	D[22]	IOGT*	
24	BD[7]	D[23]	IORQ*	
25	BD[6]	D[24]	BL*	
26	BD[5]	D[25]	0V	
27	BD[4]	D[26]	CLK2	
28	BD[3]	D[27]	CLK8	
29	BD[2]	D[28]	REF8M	
30	BD[1]	D[29]	0V	
31	BD[0]	D[30]	DBE	
32	0V	D[31]	0V	

Table 10.4 : Main PCB connector

Loading of the podule bus

Each podule may present one load to the podule bus signals CLK2, CLK8 and REF8M. Each podule may present two loads to other signals on the podule bus, where the load may be either HC, HCT, LS, ALS or F series logic. The use of HCMOS logic is highly recommended. When driving the data bus from a podule, care should be taken not to overdrive the bus. Series resistive termination of these lines with about 68 Ohms is recommended.

Signal standards

All signals from the main PCB to the podules are CMOS logic levels. Podules may drive the bus with TTL logic levels, but CMOS logic levels are recommended.

Power

Voltages available on the podule connector are -5 V, +5 V and +12 V. In normal cases podules should take no more than the following current from any one rail:

Rail	Total	Per Slot
5 V	4.5 A	1.5 A
12 V	0.7 A	0.7 A
-5V	0.5A	0.5A

10:4 Podule identity

Each podule must be capable of identifying itself to the host operating system, and this is done by means of the podule identity (PI). It consists of at least one byte (the low byte) of which bits 3 to 7 carry PI information, and is usually followed by several more bytes. The PI is read by a synchronous read of address 0 of the podule space.

Podule Identity space

The podule identity space starts at podule address 0 and extends into the podule space as required. The minimum PI, which all podules must support, is a single readable byte at address 0, called the PI low byte. Most podules will support an extended PI which consists of eight bytes starting from address 0. The PI (whether extended or not) must appear at the bottom of the podule space, from address zero upwards after reset. It does not however have to remain readable at all times, so it can be in a paged address space so long as the podule is set to page zero on reset. Refer to the sections *Podule interrupts* and *FIQ and IRQ status* below. This has the effect that the PI, including the podule present bit, is only valid after reset until the podule driver is installed.

The first 16 bytes of the podule identity space is assumed to be bytewide only. The space after this may be 8, 16 or, in the future, 32 bits wide. Bits 2 and 3 in byte 1 of the extended PI (W0, WI) indicate the width of the code (if any) which follows. If the PI is included in a ROM which is 16 or 32 bits wide, then only the lowest byte in each half-word or word must be used for the first 16 (half) words.

Code space

In addition to the podule identity, which all podules must support, a podule can contain code or data in ROM. In the Arthur operating system environment, this is typically used for driver code for the podule, and is downloaded into system memory by the operating system before it is used. Often this code will be in a paged address space. The manner in which this code is accessed is variable and so it is accessed via a loader. The format of the loader is defined for each operating system, and gives access to a paged Address space. The loader must live in the podule space above the PI after reset, the position and size of it being defined by a chunk directory entry. Note that the PI and the loader may themselves be in the paged address space as long as they appear at address zero after reset. Refer to the section *Chunk directory structure* below.

Podule Identity low byte

In the UNIX environment, device installation is more complex, and this mechanism is currently not used.
The low byte of the PI is as follows:

7	6	5	4	3	2	1	0
A	ID[3]	ID[2]	ID[1]	ID[0]	FIQ	P	IRQ

IRQ = 0 : not requesting IRQ) see text
= 1 : requesting IRQ)

P = 0 : podule is present

FIQ = 0 : not requesting FIQ) see text
=1 : requesting FIQ)

ID[3:0] = 0 : extended PI
<> 0 : ID field

A = 0 : Acorn conformant podule
= 1 : non-conformant podule

Podule presence

The host operating system has to know if there are any podules present. Normally BD[1] is pulled high by a weak pullup. Reading the low byte of the PI will therefore read a 1 on this bit unless a podule is present. All podules must have bit 1 low in the low byte of the PI.

Podule Interrupts

A podule which is capable of generating a PIRQ* or a PFIQ* MUST carry a status bit for each of these interrupt sources. These two status bits must be in the low byte of the PI unless the podule contains an extended PI in which case the status bits may be relocated in the podule address space. A podule which is holding PIRQ* low must set bit 0 high in the low byte of the PI. A podule which is holding PFIQ* low must set bit 2 high in the low byte of the PI. In this way the operating system can quickly find which podule is generating the interrupt.

If the podule contains paged ROM, these status bits may be located elsewhere in the podule address space, in which case the two bits in the PI low byte should be zeros. The location of these status bits must appear in the ROM space above the extended PI. See the section *Interrupt status pointers* below.

If a podule is not capable of generating either a PIRQ* or a PFIQ* then bits 0 and/or 2 in the low byte PI must be zero. If the interrupt status bits have been relocated, then the respective position mask should be set to zero. Refer to the section *Interrupt status pointers* below.

ID field

There are four bits in the low byte of the PI (BD[3:6]) which may be used for podule identification. These should only be used for the very simplest of podules or temporarily during development. Most podules should implement the extended PI which eliminates the possibility of podule IDs clashing. When an extended PI is used, all four bits in the ID field of the low byte PI must be zero.

Acorn conformance bit

The most significant bit in the low byte of the PI must be zero for podules that conform to this Acorn specification.

Identification extension

If the ID field of the low byte of the PI is zero then the PI is extended. This means that the next seven bytes of the PI will be read by the operating system. The extended PI starts at the bottom of page 0 of the paged identity space, and consists of eight bytes as defined below. If bit 0 of byte 1 is not set then the extended PI is just eight bytes long. If bit 0 of byte 1 (CD) is set, then a chunk directory follows the interrupt status pointers.

7 6	5	4	3	2	1	0		
C[7]	C[6]	C[5]	C[4]	C[3]	C[2]	C[1]	C[0]	0x1C
M[15]	M[14]	M[13]	M[12]	M[11]	M[10]	M[9]	M[8]	0x18
M[7]	M[6]	M[5]	M[4]	M[3]	M[2]	M[1]	M[0]	0x14
P[15]	P[14]	P[13]	P[12]	P[11]	P[10]	P[9]	P[8]	0x10
P[7]	P[6]	P[5]	P[4]	P[3]	P[2]	P[1]	P[0]	0x0C
R R	R	R	R	R	R	R	0x08	
R R	R	R	W[1]	W[0]	IS	CD	0x04	
A 0	0	0	0	F	0	I	0x00	

A = 0 : Acorn conformant podule
= 1 : non-conformant podule

F = 0 : not requesting FIQ - see text
= 1 : requesting FIQ

I = 0 : not requesting IRQ - see text
= 1 : requesting IRQ

R = 0 : mandatory at present
= 1 : reserved for future use

CD = 0 : no chunk directory follows
= 1 : chunk directory follows interrupt status pointers

IS = 0 : interrupt status appears in low byte PI
= 1 : interrupt status has been relocated

W[1:0] = 0 : 8 bit code follows after byte 15 of ID
= 1 : 16 bit code follows after byte 15 of ID
= 2 : 32 bit code follows after byte 15 of ID
= 3 : reserved

C[7:0] = Country
M[15:0] = Manufacturer
P[15:0] = Product Type

Table 10.5 : Identification extension

FIQ and IRO status

If bit 1 in byte 1 of the extended PI (IS) is not set, then the interrupt status bits have not been relocated within the podule address space. In this case the FIQ and IRQ status bits must appear as bits 2 and 0 respectively in the low byte of the PI. Podules which cannot generate interrupts must drive these bits to zero. If bit 0 in byte 1 of the extended PI (CD) is not set either, then the interrupt status pointers do not need to be defined, as the operating system will not read them. If CD is set, then the interrupt status pointers should be defined to point to the respective bits in the PI low byte.

If bit 1 of byte 1 of the extended PI (IS) is set, then the interrupt status bits have been relocated within the podule space. In this case the interrupt status pointers must be defined as described in the section *Interrupt status pointers* below.

Note that if both IRQ and FIQ sources are provided by a podule, then a separate status bit must exist for each type of interrupt source, though the two status bits may appear at the same address if convenient. Refer to the section *Interrupt status pointers* below.

Country code

Every podule should have a code for the country of origin. The current allocation of country codes is as follows:

Country name	Code Value
UK	0
Italy	4
Spain	5
France	6
Germany	7
Portugal	8
Greece	10
Sweden	11
Finland	12
Denmark	14
Norway	15
Iceland	16
Canada	17
Turkey	20

Table 10.6: Country codes

Manufacturer code

Every podule should have a code for manufacturer. The current allocation of manufacturer codes is as follows:

Manufacturer	Code Value
Acorn UK	0
Acorn USA	1
Olivetti	2
Watford	3
Computer Concepts	4
Intelligent Interfaces	5
Caman Systems	6
Armadillo	7
Soft Option	8
Wild Vision	9
Anglo Computers	10
Resource	11
Allied Interactive	12
Musbury Consultants	13

Table 10.7: Manufacturer codes

Consult Acorn for further allocation of codes.

Product type code

Every podule type must have a unique number allocated to it. The current allocation of podule type codes is as follows:

Product Type	Code Value
Host Tube	0
Parasite Tube	1
SCSI	2
Ethernet	3
IBM Disc	4
RAM/ROM	5
BBC IO	6
Modem	7
Teletext	8
CDROM	9
IEEE 488	10
Hard Disc	11
ES D	12
SMD	13
Laser Printer	14
Scanner	15
Fast Ring	16
VME Bus	17
PROM Programmer	18
MIDI	19
Mono VPU	20
Frame Grabber	21
Sound Sampler	22
Video Digitiser	23
GenLock	24
CODEC Sampler	25
Image Analyser	26
Analogue Input	27
CD Sound Sampler	28
6 MIPS Signal Processor	29
12 MIPS Signal Processor	30
33 MIPS Signal Processor	31
Touch Screen	32
Transputer Link	33
Interactive Video	34

Table 10.8 : Product type codes

Consult Acorn for further allocation of codes.

Interrupt status pointers

If bit 1 of byte 1 of the extended PI (IS) is set, then the address of the FIQ and IRQ status bits must be provided in the eight bytes which follow the extended PI, even if the two status bits are at address 0. There are two sets of four byte numbers as detailed below, each consisting of a three byte address field and a one byte position *mask* field. The position mask defines which bit within the status byte refers to the status bit. It should consist of one 'one' and *seven* zeros. The other bits within the status byte may be `don't cares'. If the podule does not provide one of these interrupt sources, then the respective position mask should consist of eight zeros.

If bit 0 of byte 1 of the extended PI (CD) is set, then bit 1 of byte 1 of the extended PI (IS) must be set and hence the addresses must be present.

Note that these eight bytes are always assumed to be bytewide. Only the lowest byte in each word should be used. After byte 15 (address 40H upwards), wider words may be used, according to the setting of W[1] and W[0] in the extended ID. See the section *Identification extension* above.

The 24 bit address field allows for an absolute byte address with an offset from 0x3000000 to be clef-med. Hence the cycle speed to access the status register can be included in the address (encoded by bits 19 and 20). Bits 14 and 15 should be zero.

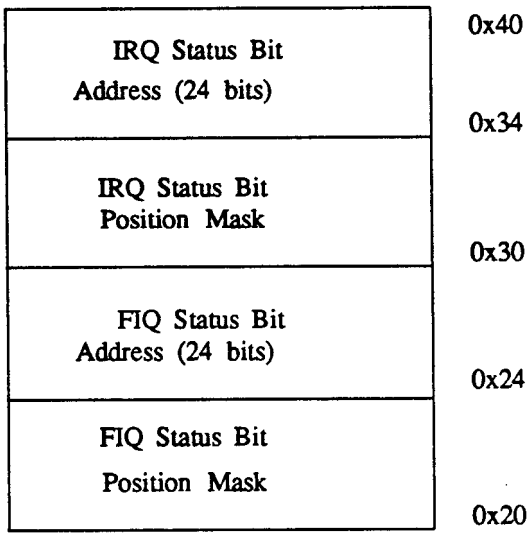


Figure 10.5 : Interrupt status pointers

Chunk directory structure

If bit 0 of byte 1 of the extended PI (CD) is set, then following the interrupt status pointers is a directory of chunks of data and/or code stored in the ROM. The lengths and types of these chunks and the manner in which they are loaded is variable, so after the eight bytes of interrupt status pointers there follow a number of entries in the chunk directory. The chunk directory entries are eight bytes long and all follow the same format. There may be any number of these entries. This list of entries is terminated by a block of four bytes of zeros.

Note that from here on the definition is in terms of bytes. If the podule supports a 16 (or in the future 32 bit) wide interface then the operating system must take this into account.

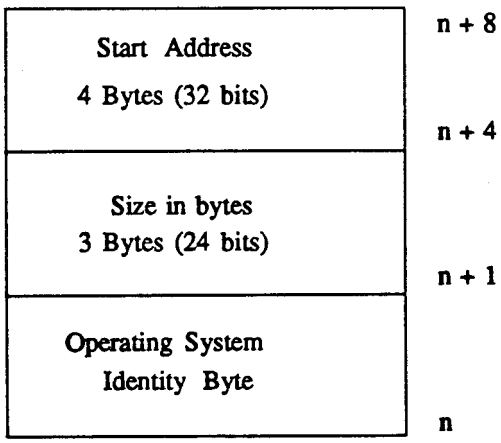


Figure 10.6: Chunk directory structure

One of these blocks must be the code loader. It contains the code to load bytes from the (paged) ROM into main memory, and as such is capable of updating the page register as required. There may be more than one loader present, to cater for different operating systems. All the loader code must be accessible after reset. After the loader is transferred to main memory, all further chunks are transferred via the loader. The chunks are again referenced by chunk directory as above, starting at a virtual address of zero. Note that after the loader has been loaded, the main podule ID area may be mapped out. An example of a typical use of the chunk directory is shown in the figure below. The shaded areas refer to chunks which are transferred via the loader.

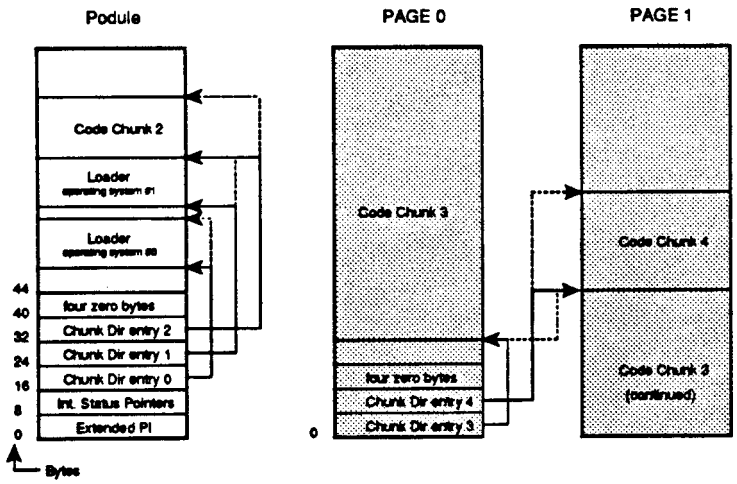


Figure 10.7 : Chunk directory structure

Operating system Identity byte

The operating system identity byte forms the first byte of the chunk directory entry, and determines the type of data which appears in the chunk to which the chunk directory refers. It is defined as follows:

7	6	5	4	3	2	1	0
OS[3]	OS [2]	OS [1]	OS [0]	D[3]	D[2]	D[1]	D[0]

OS[3] = 0 reserved
OS[3] = 1 mandatory at present

OS[2:0] = 0 Acorn Operating System #0 Arthur
D[3:0] = 0 loader
1-15 operating system dependent

1 Acorn Operating System #1
D[3:0]= 0 loader
1-15 reserved

2 Acorn Operating System #2
D[3:0] = 0 loader
1-15 reserved

3-5 reserved
D[3:0] = 0-15 reserved

6 manufacturer defined
D[3:0] = 0-15 manufacturer specific

7 device data
D[3:0] = 0 link
(for 0, the object pointed to is another directory)
1 serial number
2 date of manufacture
3 modification status
4 place of manufacture
5 description
6 *part* number
(for 1-6, the data in the pointed-to location contains the ASCII string of the information.)
7-15 reserved

Table 10.9 : Operating system identity byte

Examples of use

The previous paragraphs explained the system of podule identification. You do not need to use all of these features on all podules, and the implementation depends on the needs and complexity of the podule in question. All podules must implement at least the simplest form of podule identification. Synchronous cycles are used by the operating system to read and write any locations within the PI space (to simplify the design of synchronous podules).

Non-extended podule Identity

This is the simplest possible podule identity mechanism: It may be used for temporary podules or where podules are used in a localised, closed environment. It should not be used for podules for general sale. Non-extended PIs do not need R/W factored into their enable, as the operating system will only read the PI space.

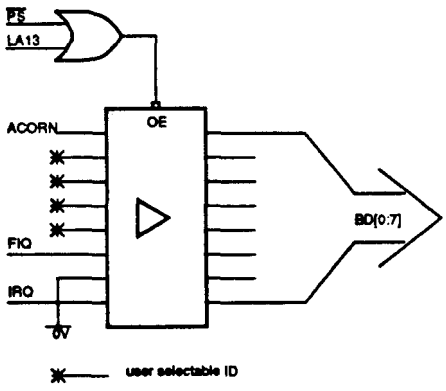


Figure 10.8 : Non-extended podule ID

Extended podule identity

The next simplest case which most podules should implement as a minimum is the case of an extended PI but no code in ROM. This can be achieved by a 32 X 8 bit PROM. An example is in the figure below.

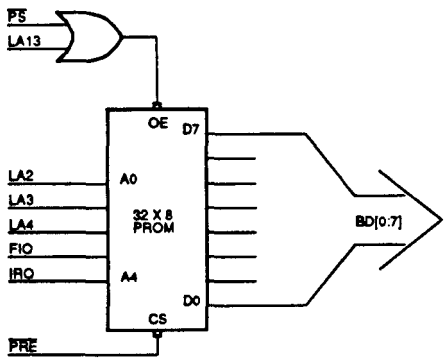


Figure 10.9 : Extended podule ID

Extended podule Identity with paged ROM

When the podule includes driver code in ROM, there are several possibilities for implementing the PI. One example showing an EPROM with a paging register is shown in the figure below. Simplifications can be made where there is only one page, or where a larger EPROM allows the inclusion of the low byte of the PI. (FIQ and/or IRQ can be factored into the address space as in the previous example).

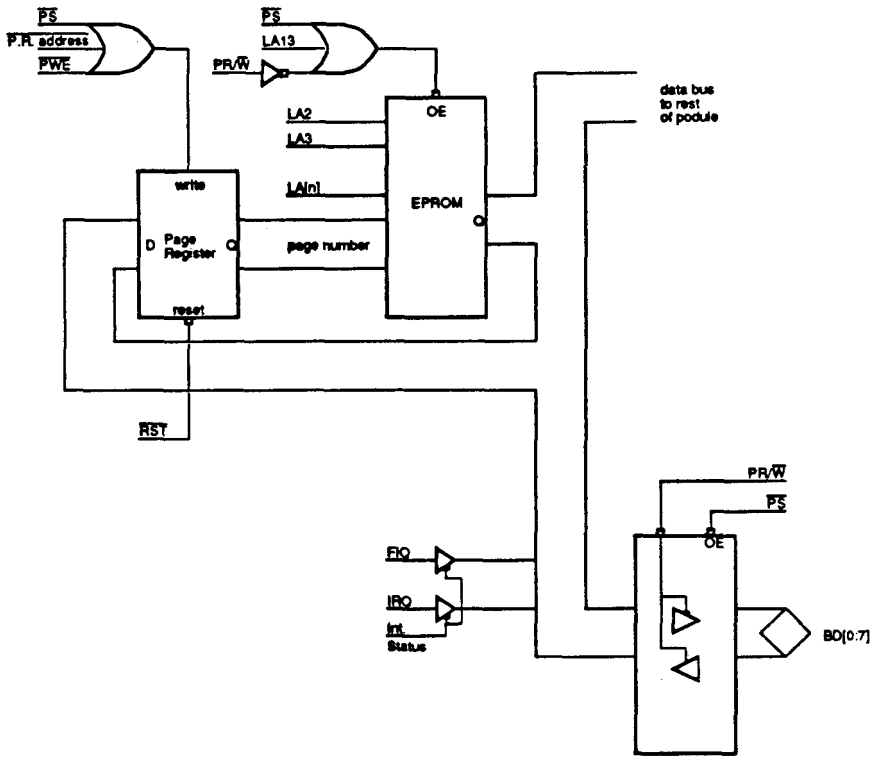


Figure 10.10 : Extended PI with paged ROM

10.5 Simple podules

Simple podules are controlled by the IOC. These podules may be accessed by one of four types of cycle, designated slow, medium, fast, and synchronous. The cycles are mapped at different addresses.

Once the cycle has started, MEMC may deassert IORQ* (and hence IOC will deassert RBE*) in order to carry out memory refresh or DMA operations. This is indicated by the shaded area in Figure 10.11 below. If, when the IOC has finished the cycle, the MEMC has not reasserted IORQ* then the I/O cycle will be stretched until the MEMC is ready to complete the cycle. This does not however alter the cycle the podule sees, because the cycle is in effect finished before the stretching takes place. In the case of a write the WBE* and PS* have already been deasserted, in the case of a read the data from the podule has already been latched into the data buffers by BL* :

Figure 10.11 below shows how the IOC generates a fast podule read: the IOC generates the podule read, write and select strobes, and also controls also controls the IOGT* and BL* signals. The podule read, write and select signals are timed with respect to the signal CLK8 **and NO relationship between REF8M and CLK8 can be assumed:**

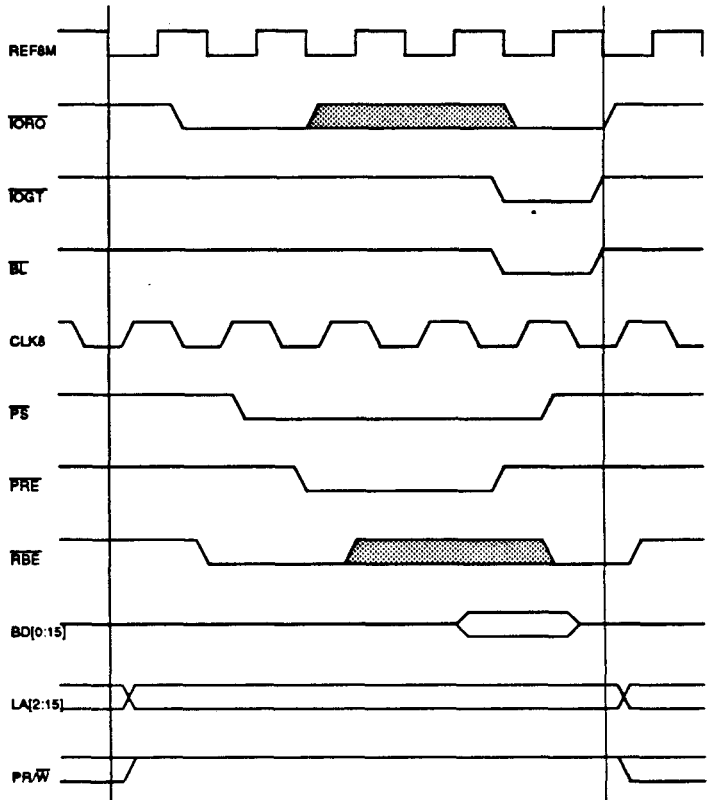


Figure 10.11 : IOC driving a podule read cycle

Note : Shaded areas; refer to text above.
The figure below shows the same cycle, but this time the MEMC has deasserted IORQ* at the time when the IOC is about to finish the cycle. Accordingly, the cycle is stretched by one 8 MHz clock period (the shaded region), but note that the access to the podule has not been stretched.

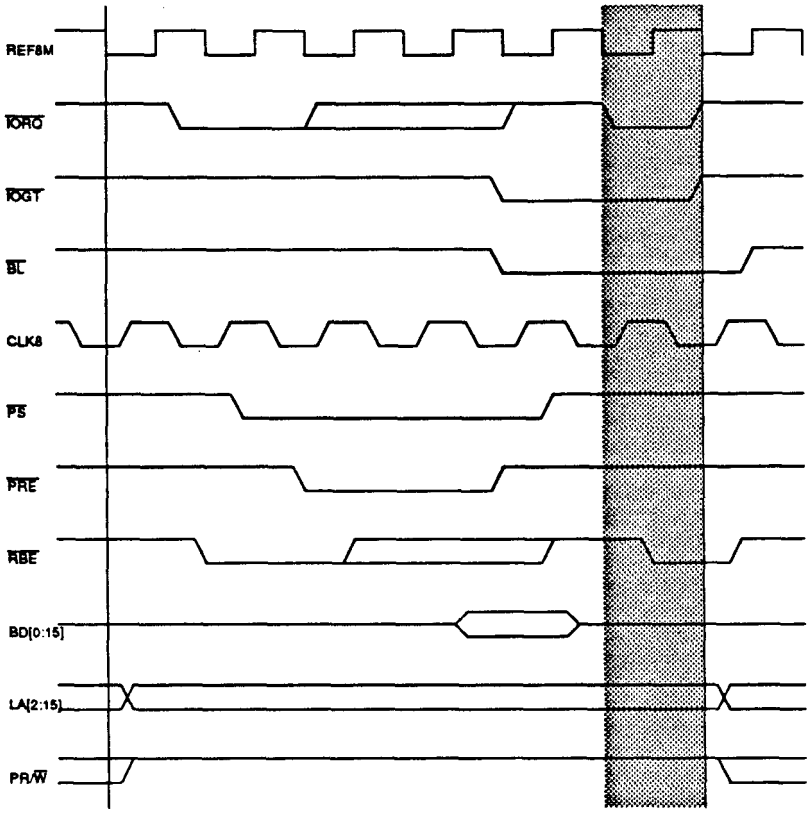


Figure 10.12: Stretched podule read cycle

Podule accesses

The following diagrams detail the four possible types of IOC podule access. In each diagram REF8M is shown, but this is only for reference. The phase relationship of REF8M and CLK8 is NOT guaranteed.

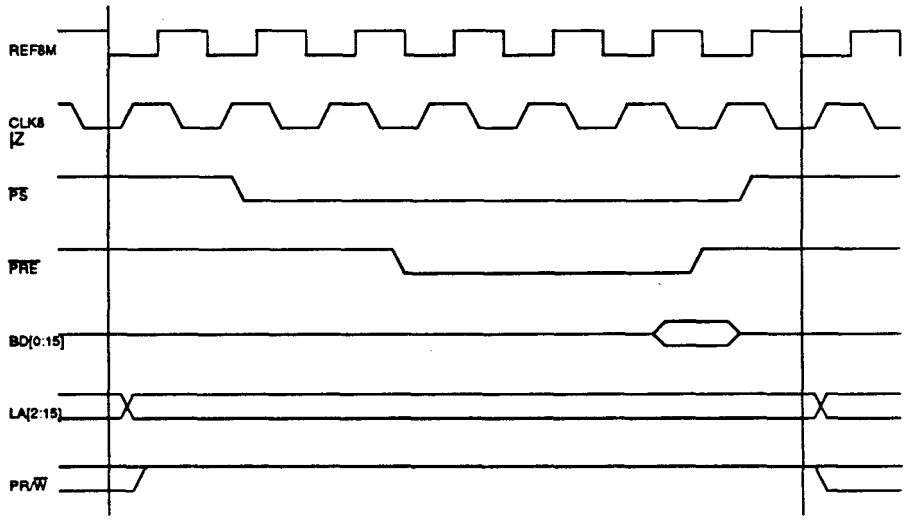


Figure 10.13 : Slow cycle read

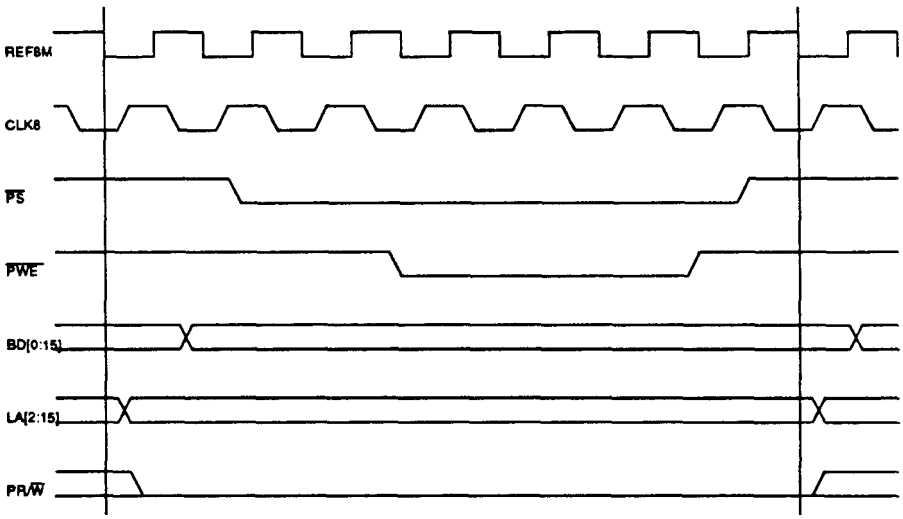


Figure 10.14: Slow cycle write

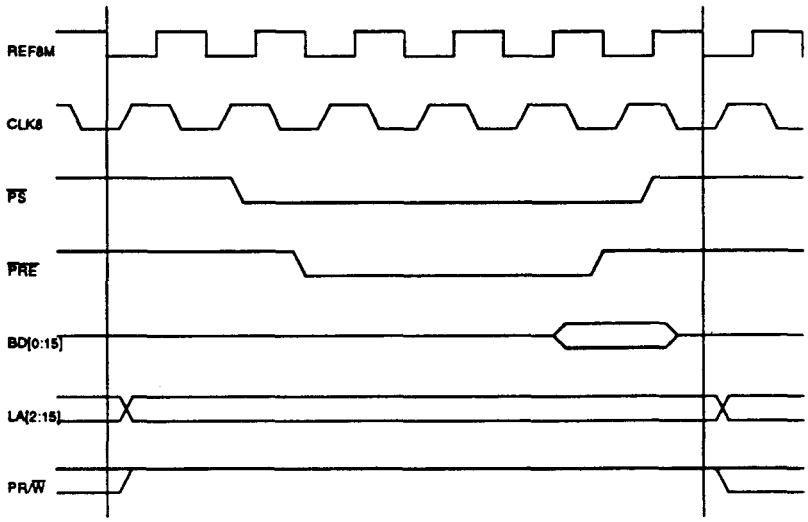


Figure 10.15 : Medium cycle read

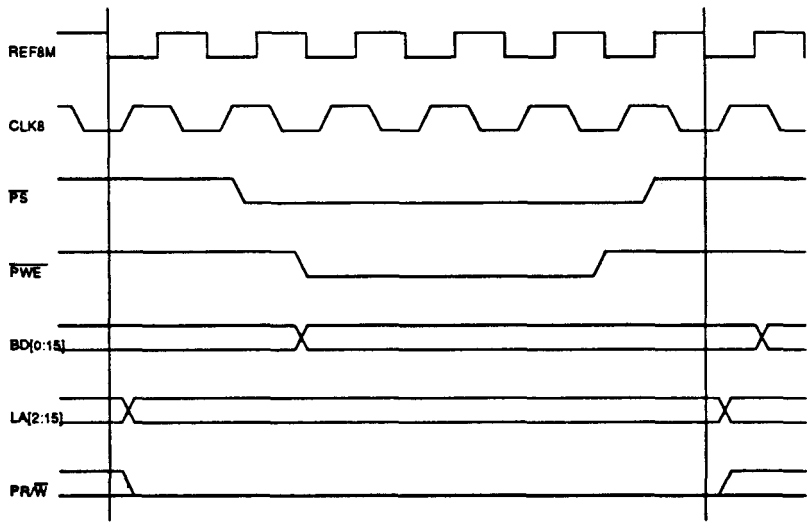


Figure 10.16: Medium cycle write

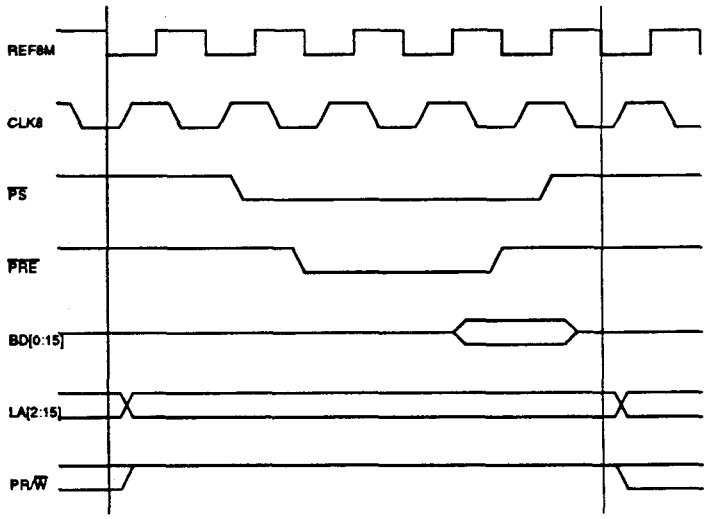


Figure 10.17: Fast cycle read

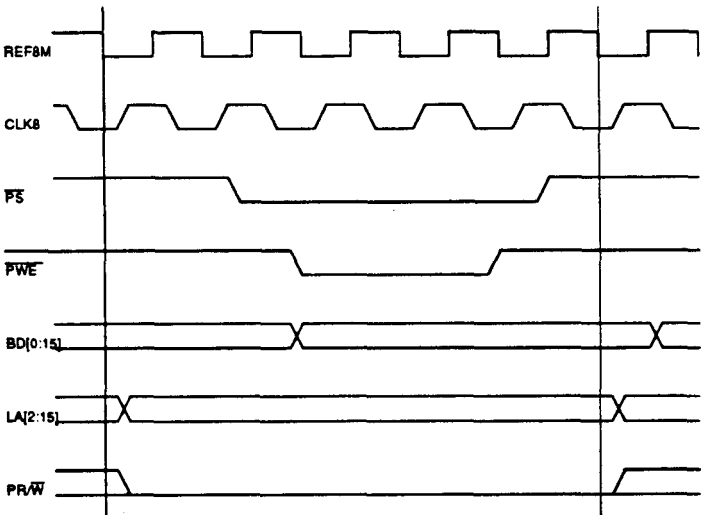


Figure 10.18: Fast cycle write

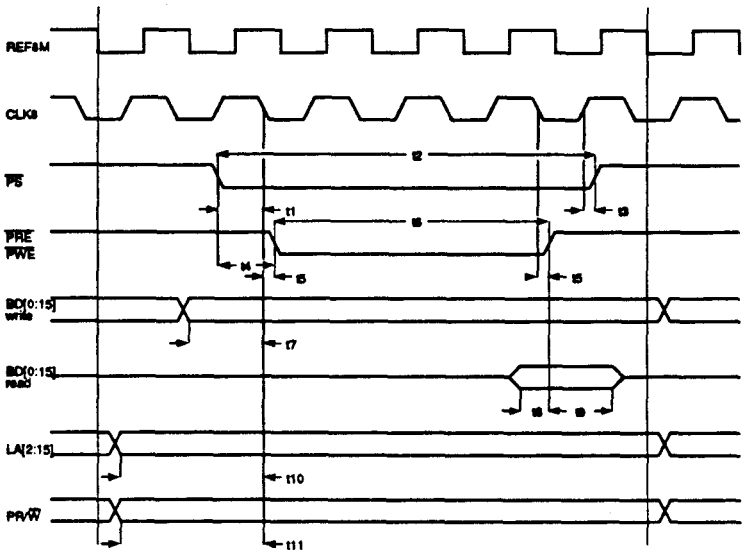


Figure 10.19 : General timing for slow, medium and fast cycle types

Note : REF8M is shown here for reference only. Do not assume any phase relationship between REF8M and CLK8.

Sym	Parameter	Min	Nom	Max	Units	Note
t1	PS* setup to CLK8	40		120	ns	
t2	PS* width TYPE slow		625		ns	
12	PS* width TYPE med		500		ns	
t2	PS* width TYPE fast		375		ns	
t3	PS* hold from CLK8	0		50	ns	
t4	PS* to PRE*/PWE* TYPE slow		187		ns	
t4	PS to PRE*/PWE* TYPE med/fast		62		ns	
t5	PRE*/PWE* delay from CLK8	0		15	ns	
t6	PRE*/PWE* width TYPE slow/med		375		ns	
t6	PRE*/PWE* width TYPE fast		250		ns	
t7	write data setup to CLK8	100			ns	
t8	read data setup to PRE*	20			ns	
t9	read data hold from PRE *	15			ns	
t10	address setup to CLK8	150				
t11	PR/W* setup to CLK8	140			ns	

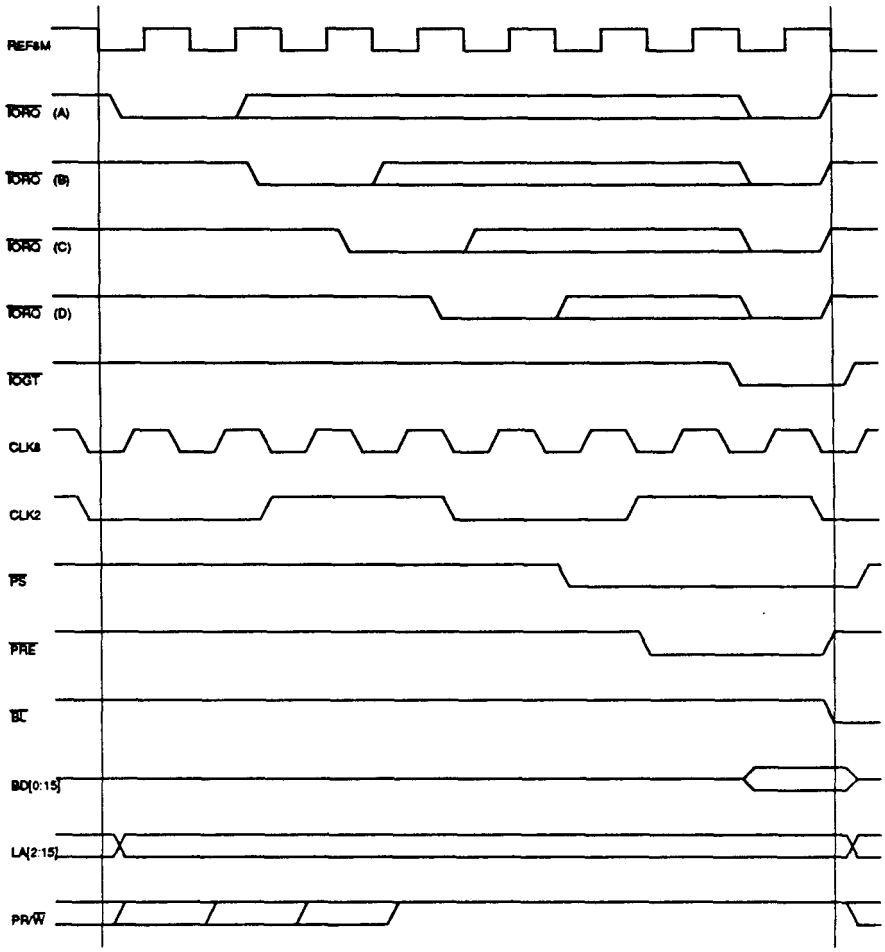


Figure 10.20: Synchronous cycle read

Note : (A) (B) (C), (D) refer to the four possible cases to allow for synchronisation to the CLK2 signal.

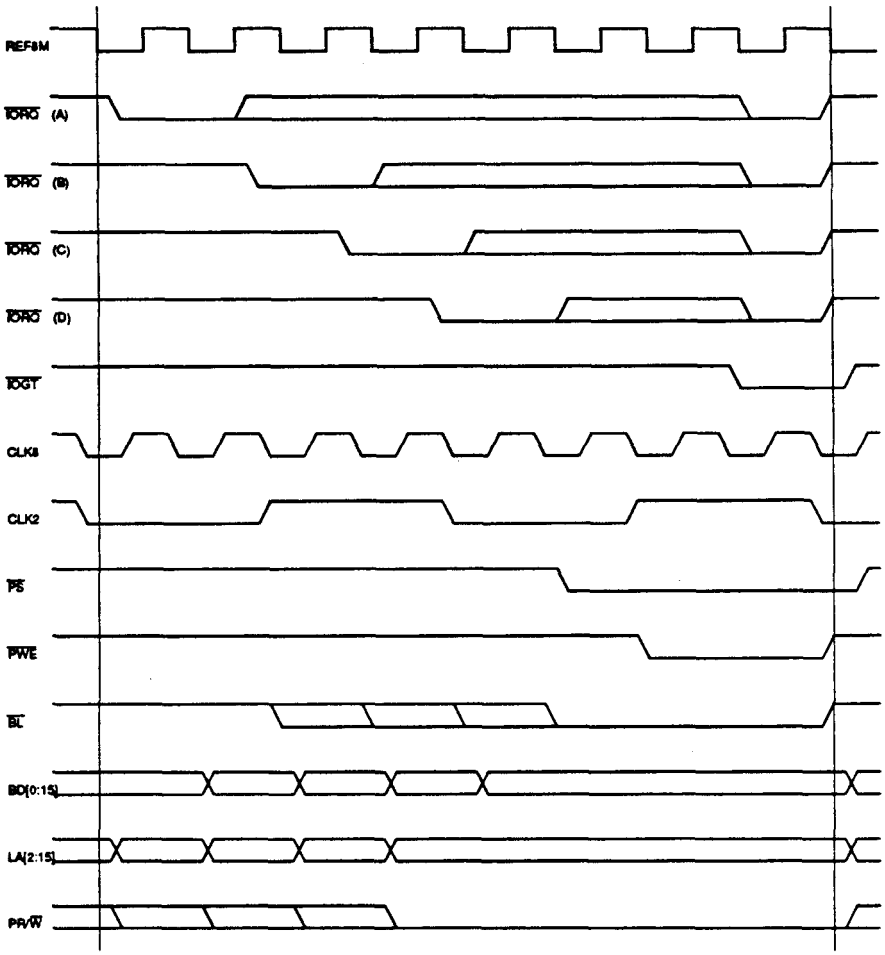


Figure 10.21 : Synchronous cycle write

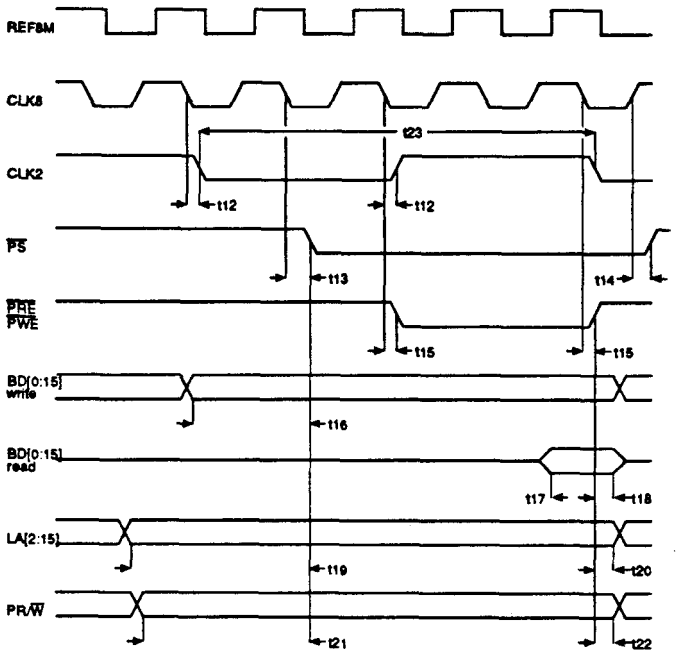


Figure 10.22 : Timings For synchronous cycle types

Sym	Parameter	Min	Nom	Max	Units	Note
t12	CLK2 delay from CLK8	0		15	ns	
t13	PS* delay from CLK8	5		50	ns	
t14	PS* hold from CLK8	10			ns	
t15	PRE*/PWE* delay from CLK8	0		15	ns	
t16	write data setup to PS*	100			ns	
t16a	write data hold from PWE*/CLK2	20			ns	
t17	read data setup to PRE*/CLK2	50			ns	
t18	read data hold from PRE*/CLK2	15			ns	
t19	address setup to PS*	150			ns	
t20	add. hold from PRE*/PWE*/CLK2	10			ns	
t21	PR/W setup to PS*	140			ns	
t22	PR/W* hold from PRE*/PWE*/CLK2	10			ns	
t23	cycle time square wave			500	ns	

10:6 MEMC podules

MEMC podules are not controlled by IOC. They share the same interface with MEMC as does the IOC, and therefore have to time their own cycles, by their I/O controller. This interface has two control lines, IORQ* (driven by MEMC) and IOGT* (driven by the podule or IOC). IOGT* is an open drain signal allowing multiple devices to sit on this interface. MEMC podules are decoded by LA[21) low, and IOC is decoded by LA[21] high. But even when IOC is not selected, it continues to control the external buffer enables, RBE* and WBE*. The latching of the buffer must however be controlled by the podule which is controlling the cycle. This is done by pulling BL* low, and is also an open drain signal.

I/O controller Interface

I/O controllers use a handshaking system to synchronise I/O peripherals with the system data bus. The interface is timed with respect to the REF8M clock, and cycles may be produced in multiples of 8 MHz clock ticks. When the processor accesses the I/0 controller address space (while MEMC is in supervisor mode), MEMC starts an I/O cycle by driving IORQ*, low and holding the processor clocks (stretching the processor cycle when PH2 is high). The I/O controller signals that it is ready to end the I/0 cycle by driving IOGT*, low. The I/0 cycle are seen low on the rising edge of REF8M, with MEMC driving IORQ* high and releasing the processor clocks, and the I/0 controller driving IOGT* high on the next falling edge of REF8M.

An I/O cycle is shown in the figure below. The cycle starts with IORQ* being taken low. There follows a number of 8 MHz clock ticks until the I/O controller is in a position to complete the cycle. The IOGT* line is taken low, and both MEMC and the I/O controller see IORQ* and IOGT* low on the rising edge of REF8M, so the I/O cycle terminates on the next falling edge of REF8M.

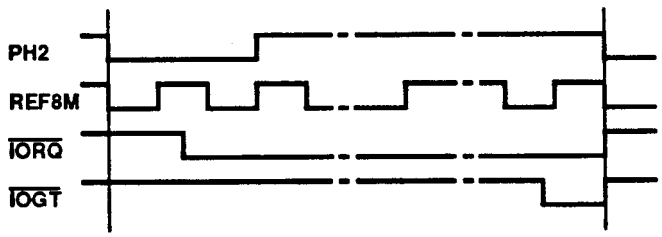


Figure 10.23: I/O cycle

Some I/0 cycles may only take 250 ns as shown in Figure 10.24 below. To give the I/O controller adequate time to recognise such operations, MEMC produces the first IORQ* early in the I/0 cycle.

The extension of IORQ* only happens at the start of an I/O cycle; if the IORQ* signal is removed during a DMA or refresh operation, it will be reasserted when REF8M goes low.

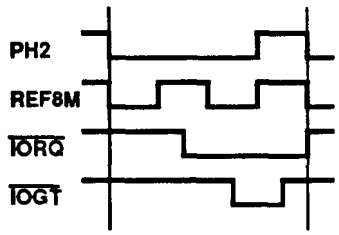


Figure 10.24 : Fast I/O cycle

I/O cycles may be interrupted by DMA and refresh operations, as shown in the figure below. If a DMA or refresh operation is pending, the IORQ* signal is driven high when REHM next goes low. The DMA/refresh operation may then begin, and when it completes, the I/O cycle is resumed by setting IORQ* low (provided no more DMA or refresh operations are pending). The DBE line is always driven low during DMA/refresh operations to disable the processor data bus drivers. Hence the I/O cycle is stretched, and the write data would become invalid in the middle of the cycle. The data must therefore be latched into the data bus buffers by the I/O controller during the first IORQ* low period, and be held until the I/O cycle has completed. This is done by the I/O controller driving BL* low for this period. The maximum time for which an I/O cycle may be interrupted in this way is 1875 ns (ie fifteen 8 MHz cycles).

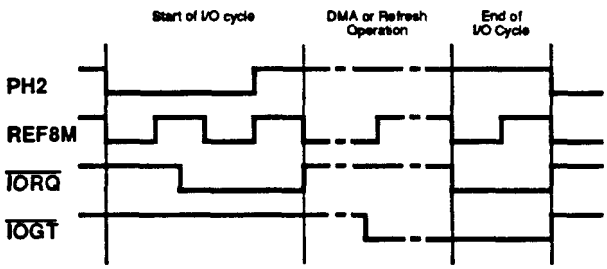


Figure 10.25 : I/O cycle interrupted by a DMA or refresh operation

NOTE: Care must be taken not to address a non-existent I/O controller, as MEMC will hold the processor clocks indefinitely until a low is seen on the IOGT* line, or RESET is set high.

MEMC podule timing

A typical cycle with timing parameters is shown in the figure below. The sequence consists of a MEMC podule access, a DRAM refresh by MEMC, with the end of the podule access delayed by one 8 MHz clock cycle.

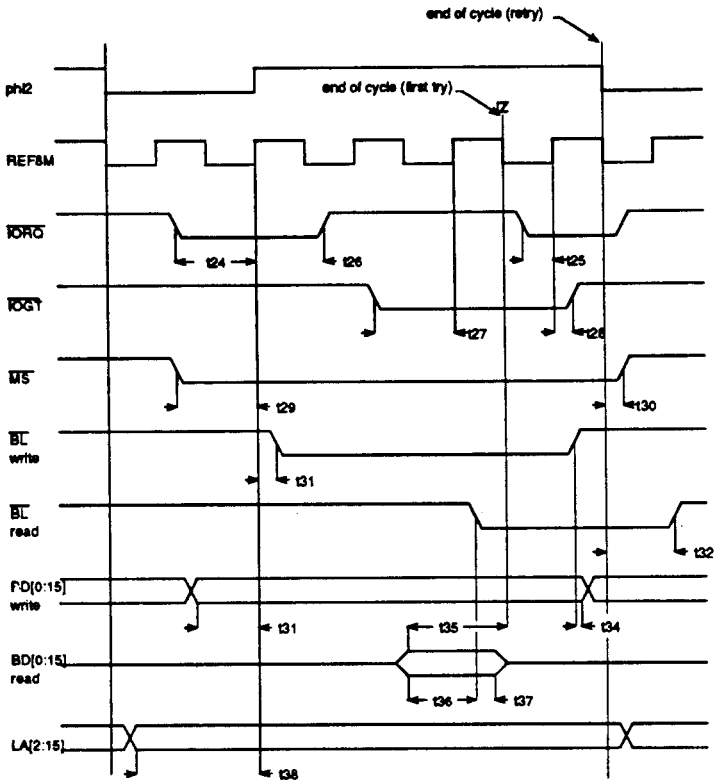


Figure 10.26: MEMC Podule timing

Sym	Parameter	Min	Nom	Max	Units	Note
t24	IORQ* setup (first attempt)	70		115	ns	
t25	IORQ* setup (retries)	50		75	ns	
t26	IORQ* hold	50			ns	
t27	IOGT* setup	25		120	ns	
t28	IOGT* hold	10		100	ns	
t29	MS* setup to REF8M	110			ns	
t30	MS* hold	5			ns	
t31	BL* delay write	0		65	ns	
t32	BL* hold read	10		100	ns	
t33	BD[0:15] setup write	85			ns	1
t34	BD[0:15] hold from BL write	5			ns	
135	BD[0:15] setup to REF8M read	50			ns	2
t36	BD[0:15] setup to BL* read	20			ns	
t37	BD[0:15] hold from BL* read	15			ns	
t38	LA[2:15], PR/W* setup to REF8M	140			ns	

Note 1 : with BL* high ie buffers transparent.
Note 2 : setup to the earliest possible end of cycle.

10:7 Backplane circuit description

Podule and module selection
S6, LA14, 15 and 21 are decoded by IC1 (74HC139) to provide:

- four podule selects PS*[0:3], and
- four module selects MS*[0:3]

LA15	LA14	Podule selects S4*=0	Module selects LA21=0	
0	0		PS0*	MS0*
0	1		PS1*	MS1*
1	0		PS2*	MS2*
1	1		PS3*	MS3*

Table 10.10 : Podule and module selects

Interrupt mask
The two PALs (IC2 and IC3) extend IOC interrupt mask/register structure to podule interrupts (PIRQs). This allows the PIRQ from each podule to be individually masked or enabled.

The two PALs are identical:
IC2 controls PIRQs from podule slots 0 and 1
IC3 controls PIRQs from podule slots 2 and 3.

PAL operation
During reset, RST* input (pin 4) is taken low, setting the mask register to l's, so enabling interrupts.

To access the registers, S6* (pin 1) is taken low, LA2 (pin5) high selects the mask register, low selects the interrupt request register.

The PIRQ input (pin 2) corresponds to the data pin 14 and the PIRQ input (pin 9) to the data pin 13. See table 5.2 in *The input/output system* for register addresses.

Chapter 11 Laser printer interface podule

11.1 Hardware overview

IC25 generates the main system clock, SYSCK, which is carefully chosen as an exact multiple of the laser video dot rate. In this case, the card is configured specifically to drive a 300 dpi CANON CX/SX print engine directly, and the system clock is 12 times the dot frequency which ensures high quality of vertical dot alignment. Two other inverters are used to buffer and invert the podule READ/WRITE* and the RESET* signals from the podule connector.

IC66 provides buffering of the NOT IORQ and the REF8M signals from the podule connector, which are time-critical signals (hence the use of a 74AC08), plus buffering of two address lines.

IC58 is a bidirectional transceiver which buffers the low eight bits of the podule data bus.

IC17 is the podule ID and code ROM; the ROM is paged into podule space; links LK1 and LK2 allow configuration of 28-pin EPROM or ROM devices of type 27128, 27256 and 27512.

IC22 is an eight bit latch which buffers the low-order podule latched address lines and which provides address hold to module address space access.

IC15, IC54 are address-mapped latches which store the 16 bit podule data to provide the demultiplexed top 16 bits of data back to a 32 bit data path used on the laser podule.

IC10 is an Acorn proprietary module address space decode PAL which provides the control signals for the mapped I/O registers on the laser podule.

IC32 is an Acorn proprietary podule interface PAL which provides the ROM paging latch, IRQ and FIQ gating and miscellaneous interface gating functions.

IC2 is the Acorn custom CMOS peripheral input/output controller, IOC, which provides interrupt control and synchronisation logic, programmable timers and input/output ports, and programmable external peripheral bus cycle and address decoding. All the laser printer interface signals are handled by IOC, as well as the video controller video request interface.

IC11 is the Acorn custom CMOS video controller, VIDC, which is a fully programmable CRT controller for bit-map displays (which in fact has full analogue video and sound DAC outputs, unused in this application). VIDC is used in hi-resolution monochrome configuration, and the clock is derived from a gated form of the synchronised laser dot clock. The device requests quad-word (4 x 32 bit) DMA data transfers (under software ' DMA' control using the ARM fast interrupts FIQ for maximum flexibility) and performs raster timing and serialisation to multiples of four bits. An external R/C circuit (R3/C3 and D1 to remove negative spikes) is used to force VIDC into a single scan-line mode, timed after the end the of displayed raster. The horizontal synchronisation period is timed to freeze the video clock until the printer signals the start of the next raster.

IC14 is an Acorn proprietary video laser interface PAL, VLASER6, which performs phase-locking to 1/12th of laser pixel period synchronous to the laser beam detect signal. It generates the clock for VIDC and synchronously bit-serialises the four bit video data to produce the laser video raster. When the controller is inactive, this PAL is in test mode and serialises data in free run mode. The design of this PAL is optimised for a very high (hundreds of years) synchronisation MTBF as the 22 MHz clock phase locks to beam detect (external asynchronous) and horizontal sync (VIDC synchronous, but for fast VIDC may be aligned to clock set-up time).

IC36 is a 75116 balanced-line transceiver which interfaces both the beam detect input from, and drives the video signal to, the printer.

IC29 is a hex Schmitt-input inverter pack, low-power Schottky rather than CMOS to preclude latch-up, which interfaces the five inputs from the printer that the laser engine uses. The vertical sync request input is re-inverted to produce a falling edge interrupt to IOC.

IC78 is a hex high-current, open-collector inverting driver, used to drive the six control lines to the printer.

11.2 Address map

The laser podule appears both in podule and module address space: reading the podule address space reads from the paged ROM, whilst reading and writing the module address space accesses the control and 'FIQ-DMA fifo' registers.

Given the podule base address (slot dependent):

(X implies illegal byte access)

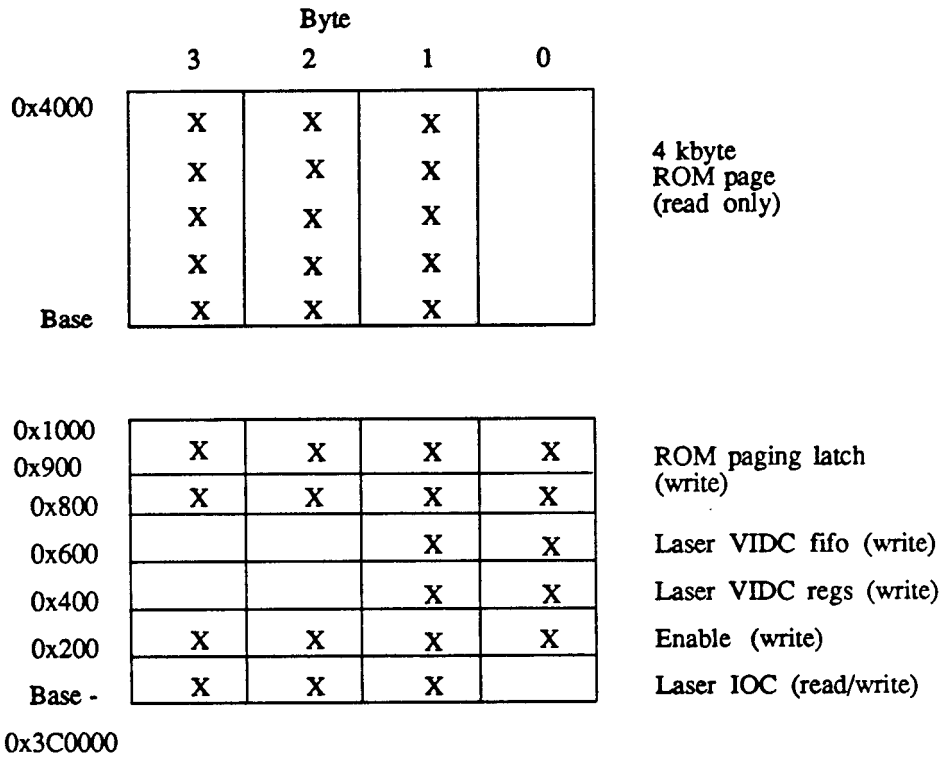


Figure 11.1: Address map

Note: the 32 bit VIDC data and control registers are accessed through the 16 bit podule interface by writing to consecutive word locations, 16 bits at a time. Programming is explained later.

Note: All module space accesses complete in one 250 ns cycle.

11.3 Control registers

The control registers, accessed relative to the module-address space base are:

0x000 Laser IOC control output port (read/write)

0x010 Laser IOC IRQ status port (read)
0x014 Laser IOC IRQ request port (read)
0x014 Laser IOC IRQ clear port (write)
0x018 Laser IOC IRQ mask port (read/write)

0x020 Laser IOC input status port (read)
0x028 Laser IOC input IRQ mask port (write)

0x030 Laser IOC FIQ status port (read)
0x034 Laser IOC FIQ request port (read)
0x038 Laser IOC FIQ *mask* port (read/write)

0x040 Laser IOC timer count (low-byte) (read)
0x040 Laser IOC timer latch (low-byte) (write)
0x044 Laser IOC timer count (high-byte) (read)
0x044 Laser IOC timer latch (high-byte) (write)
0x048 Laser IOC timer restart (write)

(other locations are normally unused - see the IOC data sheet)

0x20x Laser podule IRQ/FIQ master enable latch

0x40x Laser VIDC VIDW space: (write only)
010xxxxxx000 Latch D[31:16] into VIDC data [31:16] latch
010xxxxxx100 Write D[31:16] into VIDC [15:0]
AND write latch data into VIDC[31:16]
AND cause VIDW cycle.
The register layout is to facilitate STMIA modes.

0x60x Laser VIDC VIDAK space: (write only)
0011xxxxxx000 Latch D[31:16] into VIDC data [31:16] latch
011xxxxxx100 Write D[31:161 into VIDC [15:0]
AND write latch data into VIDC[31:16]
AND cause VIDAK cycle.
The register layout is to facilitate STMIA modes.

0x800 Paging address latch base. (write only)
1pppp0000000 where address pppp selects page 'pppp'

Table 11.1: Control registers

Laser IOC control output port

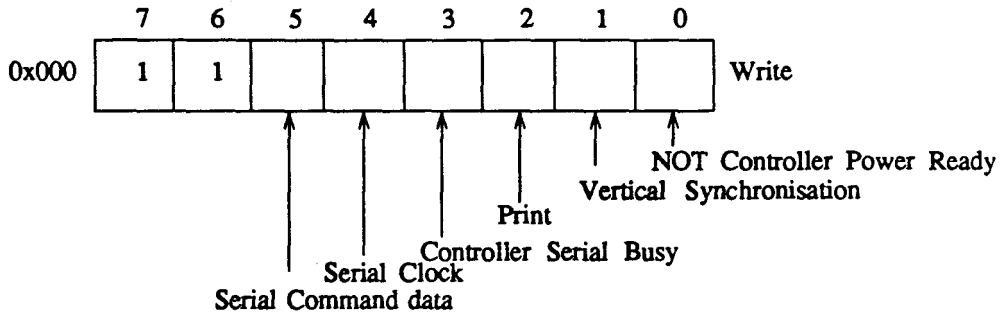


Figure 11.2: Laser IOC control output port

Setting a bit drives the interface line to the laser printer through an inverting line driver. This port resets to all bits high, with control line 0 (NOT ready) resetting the printer and setting the video phase lock circuitry in test mode (free run). (This is only of use for a manufacturing test.)

Reading this port returns the current state of the output control lines, therefore no RAM copy of the register is required.

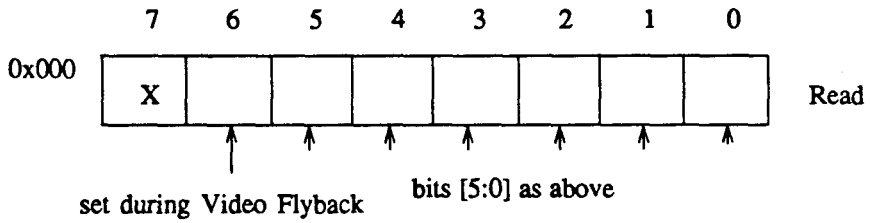


Figure 11.3 : Laser IOC control output port

Laser IOC IRQ status port

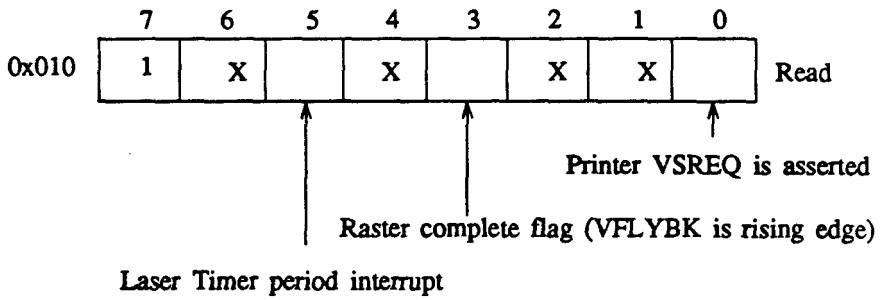


Figure 11.4: Laser IOC IRQ status port

Laser IOC IRQ request port

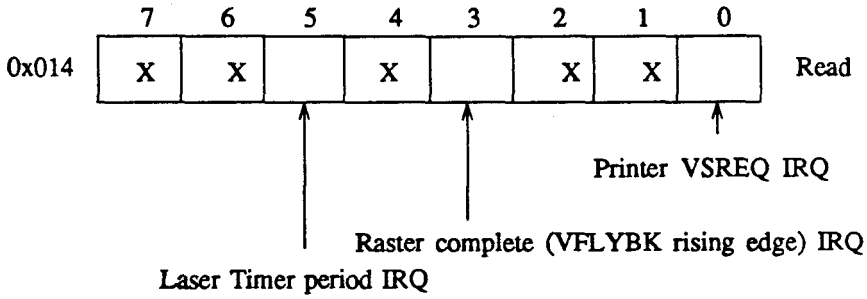


Figure 11.5 : Laser IOC IRQ request port

Laser IOC IRQ clear port

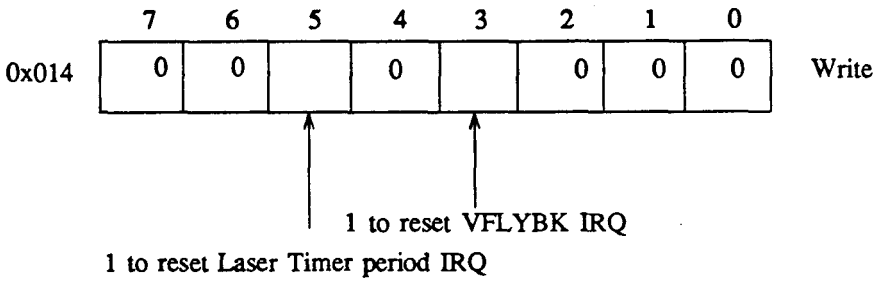
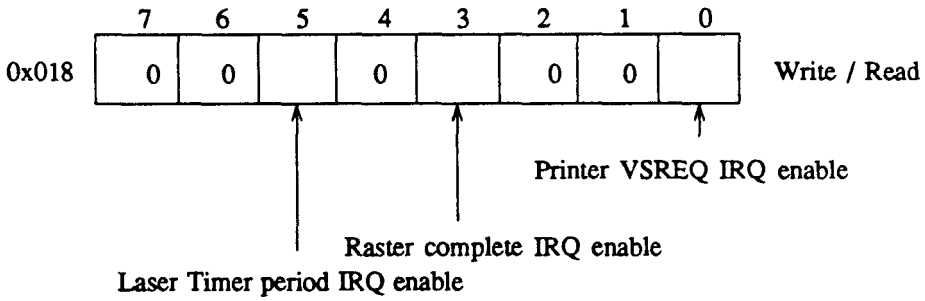


Figure 11.6: Laser IOC IRQ clear port

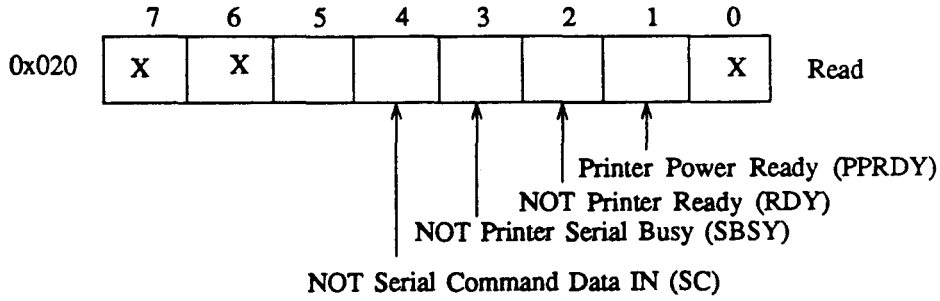
Laser IOC IRQ mask port



Note: This register is unknown after reset and should be cleared down during initialisation, prior to enabling the podule IRQ/FIQ master enable.

Figure 11.7: Laser IOC IRQ mask port

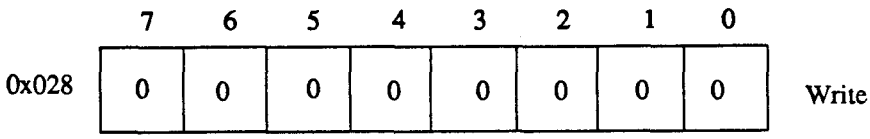
Laser IOC input status port



Note: the signals are inverted forms of the printer interface signals from the line receivers.

Figure 11.8 : Laser IOC input status port

Laser IOC input IRQ mask port



Note: This register is unknown after reset and should be cleared down cluing initialisation, prior to enabling the podule IRQ/FIQ master enable.

Figure 11.9 : Laser IOC input IRQ mask port

Laser IOC FIQ status port

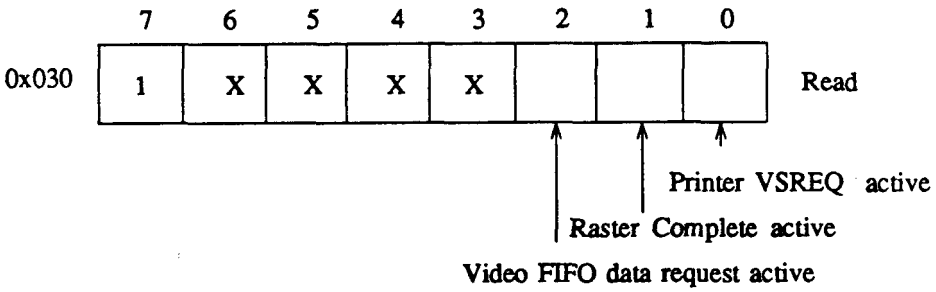


Figure 11.10: Laser IOC FIQ status port

Laser IOC FIQ request port

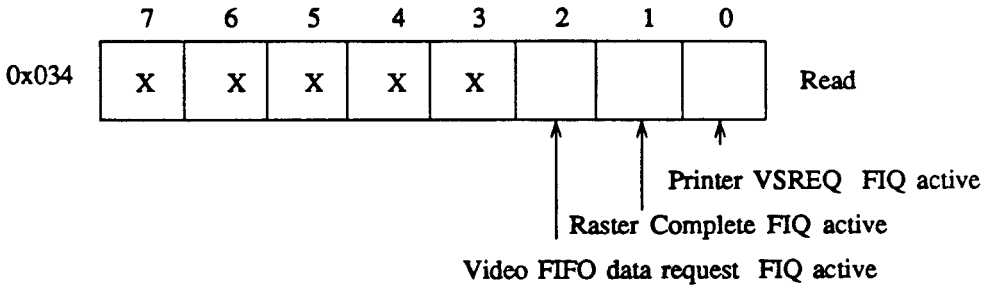
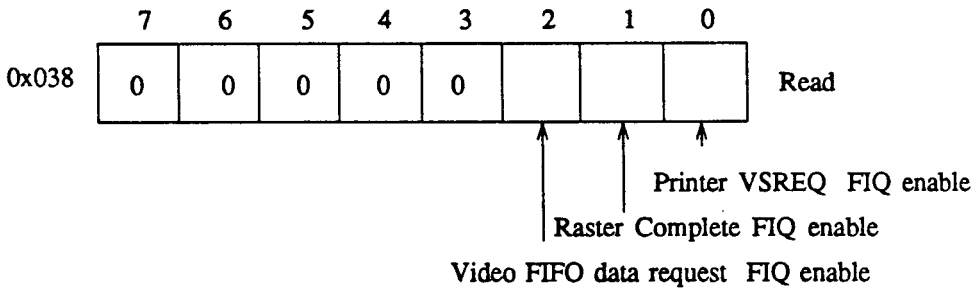


Figure 11.11 : Laser IOC FIQ request port

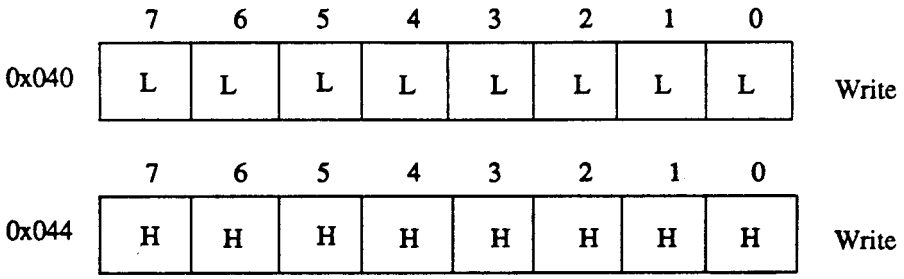
Laser IOC FIQ mask port



Note: This register is unknown after reset and should be cleared down during initialisation, prior to enabling the podule IRQ/FIQ master enable.

Figure 11.12: Laser IOC FIQ mask port

Laser IOC timer ports



Where timer interrupt period is:

binary: HHHHHHHHLLLLLLLL / 2 µS

The time is started by writing to:

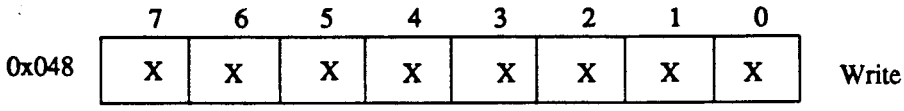


Figure 11.13 : Laser IOC timer ports

Laser podule IRQ/FIQ master enable latch
On reset the laser podule is disabled (the paging latch is cleared to zero) and the laser IOC should be initialised and the paged ROM contents copied out to RAM prior to enabling the podule.

Enabling the podule switches off ROM paging, selecting page 0 EXCEPT when a podule IRQ or FIQ is present, causing an alternate page to be switched in for the duration of the IRQ or FIQ. The switched in pages would normally be programmed with appropriate PIRQ and PFIQ bits in byte zero of the page to conform to the podule firmware specification.

To DISABLE the podule IRQ/FIQs, and allow normal paged ROM access:

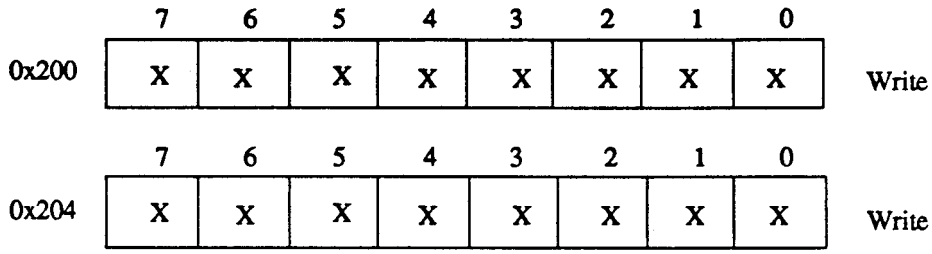


Figure 11.14 : Laser podule IRQ/FIQ master enable latch

Laser VIDC internal registers
The VIDC internal registers are accessed as 32 bit data writes strobed by the VIDW signal. The 16 bit podule interface complicates this and requires the high 16 bits to be stored in a holding latch which are written into VIDC when the low 16 bits are next output on the podule data bus. This is further complicated by the fact that to WRITE to the 16 bit podule data bus the data must be shifted to the top 16 bits of the word.

The holding latch and VIDW registers are replicated alternately to allow efficient store multiple operations to VIDW registers (MEMC la permits STM instructions to I/O space).

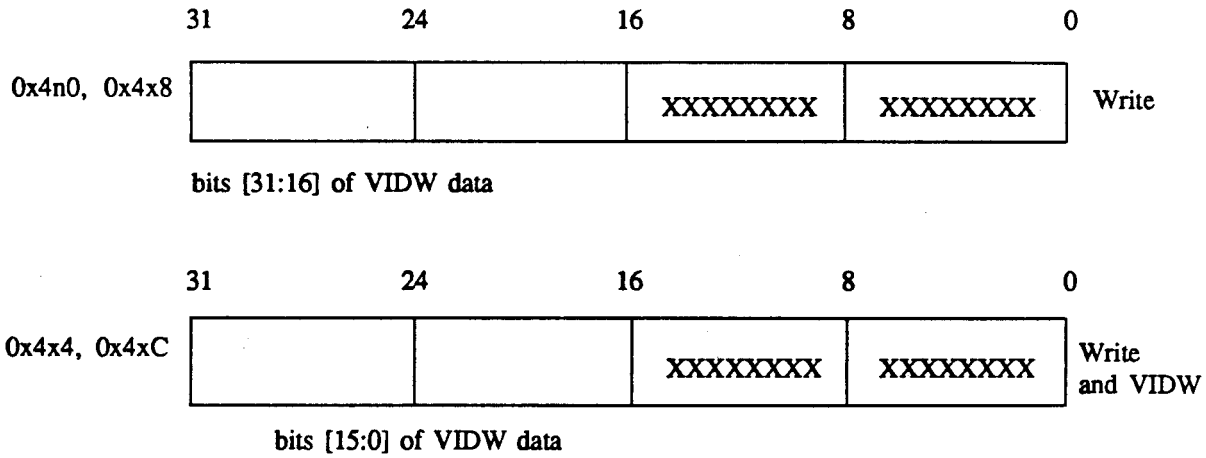


Figure 11.15 : Laser VIDC internal registers

NOTE: The Laser VIDC registers are unknown after reset and should be programmed during initialisation, prior to enabling the podule IRQ/FIQ master enable. See the VIDC data sheet for programming information.

Laser VIDC video FIFO
The VIDC internal video FIFO is eight 32 bit words deep and requests data in multiples of four words at a time. Although normally connected to a DMA controller in video applications the VIDC is configured for software handshake DMA in this application. Each video data request (VIDRQ) must be acknowledged by four 32 bit data transfer cycles (4 x VIDAK data acknowledge).

As the VIDC register case the 16 bit podule interface complicates this and requires the high 16 bits to be stored in a holding latch which are written into VIDC when the low 16 bits are next output on the podule data bus. Again the 16 bit podule data bus data must be shifted to the top 16 bits of the word. The holding latch and VIDAK registers are replicated alternately to allow efficient store multiple operations to VIDC FIFO register (MEMC la permits STM instructions to I/O space).

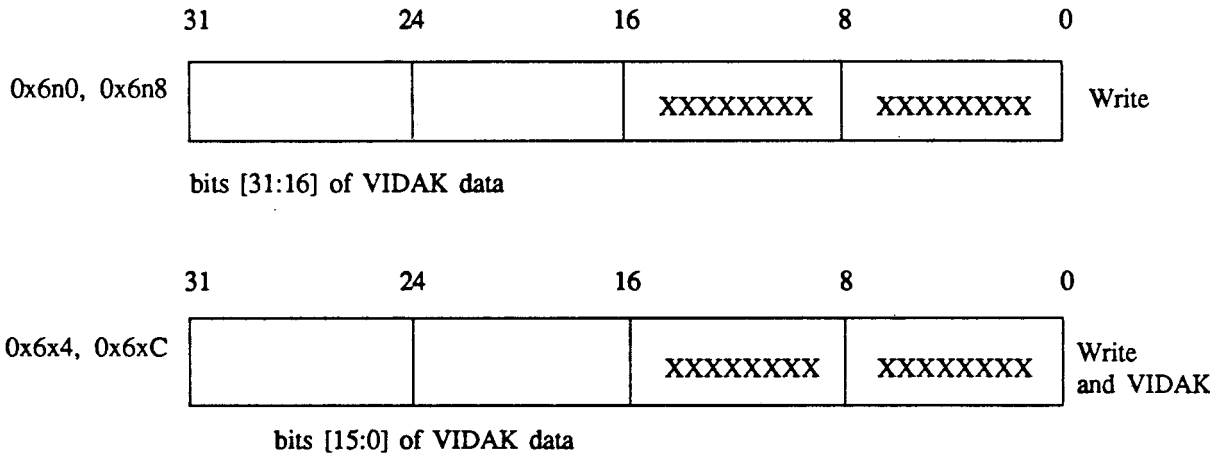


Figure 11.16: Laser VIDC video FIFO

NOTE: The laser VIDC FIFO contents are unknown after reset and should be programmed to zero during initialisation, prior to printing the border at the top of a page.

Laser ROM paging latch
The ROM appears in a 4 kbyte space in podule address-space. Page zero would normally contain the podule ID information and paging code. Page one would be paged in automatically when IRQs are enabled and present, and consecutive pages for driver handler code. Optionally page two could be used for automatic FIQ *presence* switching.

The ROM page select latch is cleared to zero on reset, and may only be modified under program control before the podule enable register is written. Address lines [10:7] are used to program the page number, but the number of pages may be limited to less than 16 if a small EPROM *is* fitted:

27128 - 16 kbyte 4 x 4 kbyte pages
27256 - 32 kbyte 8 x 4 kbyte pages
27512 - 64 kbyte 16 x 4 kbyte pages

NOTE: The ROM size is selected thus:

	LK1	LK2	
27128	A	A	- default
27256	B	A	
27512	B	B	

Thus full paging, whilst the podule is DISABLED, is achieved by writing to addresses:

0x800 - page 0
0x880 - page 1
0x900 - page 2
0x910 - page 3
0xA00 - page 4
0xA80 - page 5
0xB00 - page 6
0xB10 - page 7
0xC00 - page 8
0xC80 - page 9
0xD00 - page 10
0xD10 - page 11
0xE00- page 12
0xE80- page 13
0xF00- page 14
0xF10- page 15

The latch is WRITE only.

When the laser podule is enabled, the page latch is controlled automatically:

page 0 (NO IRQ/FIQ) (location 0 = PID + presence)
page 1 (podule IRQ active) (location 0 = PIRQ + presence)
page 2 (podule FIQ active) (location 0 = PFIQ + presence)

11.4 Canon laser printer control protocol

See the manufacturer's specification of the Canon SX printer for a description of the video interface and specification.

Power ready handshake

The printer indicates power supplies are stable and the internal controller *is* reset by asserting Printer Power ReaDY, PPRDY, signal. Once it has been stable for 2.5 seconds the laser podule may commence printer initialisation.

If PPRDY is deasserted, then all printer state is lost and initialisation must be re-commenced only when power has stabilised again.

The laser podule indicates it is active by asserting Controller Power ReaDY, CPRDY, which after 0.5 seconds is regarded by the printer as the condition to respond to the other interface signals.

De-asserting CPRDY causes the printer to unconditionally reset, expelling any paper currently in the print path, resetting all control signals and returning to the PPRDY state.

Print handshake

The printer indicates it is able to print by asserting the ReaDY control line, RDY, active low. This line indicates that the paper-paths are not jammed, paper is available and no error conditions exist. Until this signal is present the controller cannot commence printing, but may request status information through the serial secondary channel (see *Serial status channel* below).

To commence printing, the controller must assert the PRINT control line, PRNT, active low which providing the printer is ready will cause paper pre-feed and drum rotation to start. PRNT must be asserted until the printer has started printing the page (see below) and may be held asserted if multiple pages are ready for printing (to achieve the maximum page throughput rate with the next page being pre-fed whilst the last is actually printing).

The printer indicates the paper is pre-fed, the drum is rotating and the video-laser is scanning by asserting VSync REQuest, VSREQ, active low, and the controller must acknowledge this by asserting Vertical SYNC, VSYNC, active low, in response, to indicate the commitment to synchronous scan-line image transfer to the printer. The printer MUST be ready to transfer the image at this point because the printer-drum will continue to rotate until the end of the page at a fixed rate as soon as the VSYNC signal is asserted.

Video raster handshake

The laser-printer builds up the page image a horizontal scan-line at a time as the page advances at a fixed rate from top to bottom. The modulated laser beam reflecting the serial video raster is reflected off a (multi-faceted) rotating mirror which is driven by a servo-controlled motor. As the laser commences scanning of a line, a photo-detector signal produces a Beam Detect signal, BD, which provides the precise timing information for the video pixel alignment for the line. Because of the mechanical tolerances, and minor speed variation of the beam-scanning motor, the alignment of pixel data from scan-line to scan-line is critical to the print quality (especially of hatched patterns for example). Thus the leading-edge of this signal must phase-lock the pixel clock to within a minimum of one eighth of a pixel (specified by Canon) and in this design locking to one twelfth of a pixel is implemented for best results.

The controller must then leave a blank left-hand margin (programmable width to compensate for different paper widths) and then the ViDeO dot pattern, VDO, clocked out by the phase-locked oscillator from left to right. The number of pixels output depends on the image size and the width of paper used, the amount of memory reserved for the image in the controller's memory, etc.

The controller must leave a number of rasters blank at the top of the page, output the number of active rasters for the paper size, and output further blank lines at the bottom of the page for correct page appearance.

Both VDO and BD signals are time-critical and are interfaced by balanced line-drivers and receivers.

Serial status channel

There is a serial communications channel between printer and controller which is used to program certain modes in the printer (e.g. manual or cassette paper feed, etc.) and to interrogate the printer's internal status.

Serial data, transmitted on the bi-directional Serial Command interface line, SC, a bit at a time is clocked by the Serial CLocK signal, SCLK, which in this system is supplied by the controller only. (The printer can be requested to enter a mode in which it can drive the SCLK line but this mode cannot be used in this design).

Two other control lines are used to implement the serial channel handshake protocol. The controller must assert Command BuSY, CBSY, in order to indicate to the printer it is going to transfer a command or status request byte on the serial channel; when the serial data has been transmitted, the controller must wait until the printer asserts Status BuSY, SBSY. The controller must then clock out the serial data bits and check the return byte does not indicate an error in the command data status byte that was transmitted.

All four serial channel lines use active low signal levels.

11.5 Video controller programming

The video controller used is the VIDC device which *is* designed for CRT display resolutions. In this application where a typical A4 page image is built up of 8 million pixels, (for example 2432 horizontal displayed dots by 3440 vertical lines), VIDC is vertically resynchronised at the end of every line to repeatedly output a single scan line. The video display format chosen is external hi-resolution monochrome, where a four bit per pixel mode is used within VIDC but which is externally serialised by a phase-locked oscillator. The horizontal synchronisation signal from VIDC is used to indicate that VIDC is ready to start a video raster, and this signal causes the pixel-clock to VIDC to be stopped until the beam detect signal from the printer is received. The clock to VIDC is then enabled to output the horizontal sync pulse, the programmed front border and the displayed line, and uses the horizontal interlace signal to reset the vertical counters using the SINK input and then free-runs until the start of horizontal sync.

A VIDC programming table as described below should be used to initialise the internal registers; the other horizontal control registers for setting display start, display end and border end must be programmed according to the paper size and dots/raster in use.

```
VIDC Table
; fixed hi-res monochrome palette
  &    0x00000000
  &    0x04000001
  &    0x08000002
  &    0x00000003
  &    0x10000004
  &    0x14000005
  &    0x18000006
  &    0x10000007
  &    0x20000008
  &    0x24000009
  &    0x2800000A
  &    0x2C00000B
  &    0x3000000C
  &    0x3400000D
  &    0x3800000E
  &    0x3C00000F
; border blank
  &    0x40000000
; fixed horizontal
  &    0x80640000 ; HCR = fixed max
  &    0x84008000 ; HSWR = 2
  &    0x98FFC000 ; HCSR = undisplayed
  &    0x9C004000 ; HIR < display
; fixed vertical
  &    0xA0008000 ; VCR = 2 for 0,1,2
  &    0xA4004000 ; VSWR = 1
  &    0xA8004000 ; VBSR =1
  &    0xAC004000 ; VDSR = 1
  &    0xB0008000 ; VDER =1
  &    0xB4008000 ; VBER =1
  &    0xB83F8000 ; VCSR > 2
  &    0xBC000000 ; VCER illegal
; fixed control
  &    0xC0000100 ; enabled!
  &    0xE000003B ; dmarq=3, 4b/p, pixck
```

11.6 Podule Interface and laser control PAL designs

Two PALs are used in the podule design to interface the laser controller to the Acorn Technical Publishing System 16 bit podule bus and a third to form the digital phase-locked oscillator for the video raster printing. Bipolar devices were chosen essentially for low-cost and availability, but newer CMOS EPLDs of a similar speed would help cut power dissipation for the card.

Podule Interface PALS

The podule interface decoding and timing is split across two PALs. One controls the module-space access, (IOLASERm), where all the programmable device registers are mapped, and a second controls the access to podule-space where the paged ROM/EPROM is located. The second PAL also controls the IRQ, FIQ and IOGT signals to the podule backplane.

All module accesses complete in a single N-cycle.

Laser module-space decode PAL
For a definition of the laser module-space decode PAL, refer to the PAL specifications available from Acorn Computers Ltd.

Description
PAL appears in module space.

An EPROM appears in the whole of podule space, and is paged about!

The address has been carefully arranged for LDR/STR offset addressing as follows:

BAH	BA10	BA9	BA2	description
0	0	0	X	IOC (read/write, BA[6:2] reg)
0	0	1	1	ENBL (IRQ/FIQ ENBL WRITE to enable)
0	0	1	0	ENBL (IRQ/FIQ ENBL WRITE to disable)
0	1	X	0	VIDL (low 16 bit data WRITE ONLY)
0	1	0	1	VIDW (+ high 16 bit data WRITE ONLY)
0	1	1	1	VIDAK (+ high 16 bit data WRITE ONLY)
1	X	X	X	Paging latch (before ENBL set) (cleared on reset, set page number on write)

Figure 11.17: Podule interface PALs

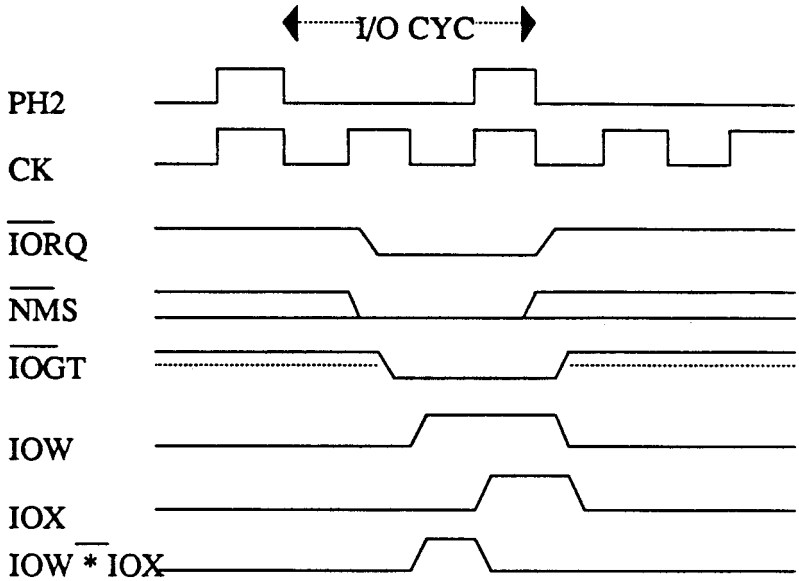


Figure 11.18 : Laser module-space decode PAL

Laser podule-space decode PAL
For a definition of the laser podule-space decode PAL, refer to the PAL specifications available from Acorn Computers Ltd.

Description
Controlled by IOLASERm PAL.

Podule space EPROM mapped as follows:

NENBL	FIQ	IRQ	X17	X16	X15	X14	
1	X	X	0	0	0	0	after reset
1	X	X	N	N	N	N	programmed page from BA[10:7]
0	1	1	0	0	0	0	enabled, no IRQ/FIQ
0	1	0	0	0	0	1	enabled, IRQ active
0	0	1	0	0	1	0	enabled, FIQ active
0	0	0	0	0	1	1	enabled, IRQ+FIQ active

Figure 11.19: Laser podule-space decode PAL

ie page 0,1,2,3 of EPROM must contain respective IRQ/FIQ bits at known location.

27128 - 16 kbyte 4 x 4 kbyte pages
27256 - 32 kbyte 8 x 4 kbyte pages
27512 - 64 kbyte 16 x 4 kbyte pages

Laser video interface PAL
For a definition of the laser video interface PAL design, refer to the PAL specifications available from Acorn Computers Ltd.

Chapter 12 Cartridge tape podule

12.1 Introduction

This chapter describes the streaming tape controller podule as used in those versions of the Acorn Technical Publishing System fitted with a streaming tape drive. The interface is basically a floppy disk controller with some special features added to enhance its ability to control a streaming tape drive. For future compatibility it is intended that this podule be capable of driving both a streaming tape drive and a floppy disk drive.

12.2 The floppy disc controller

The floppy disc controller used for this interface is the NEC µPD72067, a PC compatible device from the µPD765 family. The important features of this device are:

- ECMA/ISO and IBM DSDD format compatible
- built in digital phase-locked-loop and window signal generation running at 32 MHz. Frequency tracking ± 25%, peak shift margin 81.5%
- built in write precompensation circuitry
- CMOS.

It is not within the scope of this manual to describe this device in any detail. Reference should be made to the pPD72067 data sheet, listed in Appendix E, for all hardware and software specifications of this device.

12:3 Disk formats/ capacities

This disk controller is capable of generating, reading and writing the following formats/ densities:

IBM Formats

Data transfer rate	**Density**
125 kbps FM	Single
250 kbps FM	Single
250 kbps MFM	Double
500 kbps MFM	Quad

Data rates of 75, 150 and 300 kbps are available with the addition of a 19.2 MHz crystal to the board.

12.4 The circuit

Please refer to the circuit diagram in Appendix A whilst reading this circuit description.

Please see the PAL specifications for detailed definitions of IC66 and IC22. This is an eight bit interface and the data is buffed via IC25 (74HCT245), an octal bus transceiver. IC66 (a 16L8 PAL or GAL) handles all address decoding and drives the interrupt lines FIQ and IRQ with tri-state outputs which are enabled low when they are active. The sources of the interrupts are BUSYED for IRQs and DRQ for FIQs. INT from the FDC (IC54) is available as an input to this PAL for flexibility but is not actually used. Instead it has already been combined with the BUSYED signal from IC22. Interrupts are only possible when enabled by the INTEN signal from the control latch (IC 17) being high. IC58 (EPROM) provides up to 256 kbytes of driver firmware space accessed in 2 kbyte pages selected by the page register IC15 (74HCT273). Normally a 27128 EPROM (250 ns) is fitted to store identity information only. IC17 is an octal latch for controlling the following functions:

BIT	Signal name	Description
7	EJECT	Jumper option for disk eject signal on pin 1 of 34 way bus
6	MOTORON	Start disk drive motor
5	TC	DMA terminal count to FDC
4	FDCR	FDC hardware reset
3	INTEN	Interrupt enable
2	SETBLK	Set index pulse blocking feature (see below)
1	DENSITY	Jumper option allows program control over RWC/DENSITY signal
0	ENBS	Enable interrupts from BUSY (TRK0) edges

All signals are active high and are set low by the podule bus reset signal. (Note: The TRKO signal provided by floppy disk drives is used as a BUSY line by tape drives.)

IC22 is a 16R4 (PAL or GAL) which carries out a variety of functions:

- combines podule-bus-reset with control-latch-reset for the FDC
- allows software access to read FIQ, IRQ and BUSY signals
- blocks index pulses when indicated by the control latch signal (BIT 2)
- generates an interrupt signal (BUSYED) on all edges of the BUSY signal.

Status signal bits are:

BIT	Signal name	Description
2	FIQ	FDC DMA request pending (used for data transfer only)
1	BUSY	Read current state of BUSY line
0	IRQ	FDC interrupt request at result-phase of a command

All signals are active high.

When the SETBLK input to this PAL is low the OUTDEX output remains high allowing index signals to reach the FDC via IC11. However, when SETBLK goes high the falling edge (ie the trailing edge) of the next index pulse will cause OUTDEX to go low blocking any further index pulses to the FDC until SETBLK is cleared. This feature is only required for use with tape drives. BUSYED, when enabled by ENBSY, goes high whenever there is a rising or a falling edge on the BUSY line. This signal is combined with INT from the FDC and fed to IC66 where it will cause IRQs when enabled by INTEN. An interrupt caused by BUSYED is cleared by reading the three status bits of the PAL described above. This feature is also only required for use with tape drives.

Disk drive/tape drive control bus signals are driven by IC10 and IC2 (7438 and 7406 respectively) and received by IC32 (74HCT14 Hex inverting Schmitt trigger).

Link options

Links LK I, LK2 and LK3 cater for various size EPROMS from 64 Kbits to 2 Mbits. LK 4 enables disk drives with disk-eject functions to be used. Link options 5 and 6 allow +5 volts and +12 volts to be provided on the 34 way ribbon cable respectively. LK 7 connects the READY input of the FDC either to +5 volts or to line 34 of the control bus (via input buffer). If the disk drive uses this signal as a DISK-CHNG signal then READY must be connected to +5 volts. The DISK-CHNG **or** READY signal is also connected to the FAULT input of the FDC via the multiplexer IC14 (74HCT157)

Memory map

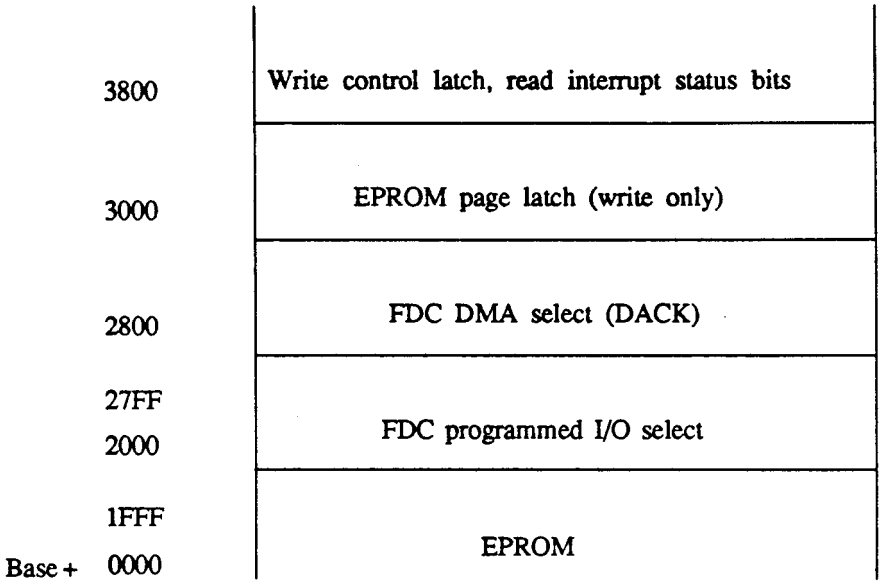


Figure 12.1 : Memory map

This podule should be accessed using fast I/O cycles although the EPROM may also be accessed using synchronous I/O cycles.

Chapter 13 Power supply unit

13.1 Introduction

The power supply unit fitted in the Acorn Technical Publishing System is a high frequency switching supply, providing 120 Watts maximum continuous output power.

The electronics hardware is printed circuit board mounted, which is fixed in an 'L' bracket with a cover. The enclosure is aluminium painted matt black.

13:2 Safety and EMI requirements

The power supply unit is approved and certified to:

UL478
CSA 22.2 Bulletin number 1402
BS58850
VDE 0806 (IEC 380),

and complies with the requirements of:

BS415
BS6301.

Electromagnetic interference susceptibility

The unit meets the radiated noise requirements of VDE0871 curve B and FCC part 15 Class B.

13.3 Specification

- Minimum efficiency at 85 W output and 240 V input is 68%
- All outputs shut down
- All outputs are protected from indefinite short circuits
- Over voltage protection on +5 V rail: between 5.8 to 7.0 V
- Hold-up time: 18 milliseconds minimum at full load 240 Vac input.

13:4 Power supply

Input voltages

Line voltage:	198 to 264 Vac RMS, frequency range 47 to 63 Hz
Link selectable:	90 to 135 Vac RMS, frequency range 47 to 63 Hz

Output voltages

There are four output rails; +5 V, +12 V, -5 V and -12 V.

Supply rail:	**+5 V**	**+12 V**
Voltage range:	Adjustable between the range 4.95 to 5.25 V dc, via trimmer located next to pin 4 on the PCB	11.3 to 12.7 V dc
Min current:	2 Amps	0.5 Amps
Max current:	12 Amps	3 Amps
Periodic and Random Deviation:	50 mV RMS over range 1 Hz to 30 MHz	100 mV RMS over range 1 Hz to 30 MHz

Supply rail:	***-5* V**	**-12 V**
Voltage range:	4.75 to 5.25 V dc	-11.3 to -12.7 V dc
Min current:	0 Amps	0 Amps
Max current:	0.25 Amps	0.5 Amps
Periodic and Random Deviation:	50 mV RMS over range 1 Hz to 30 MHz	200 mV RMS over range 1 Hz to 30 MHz

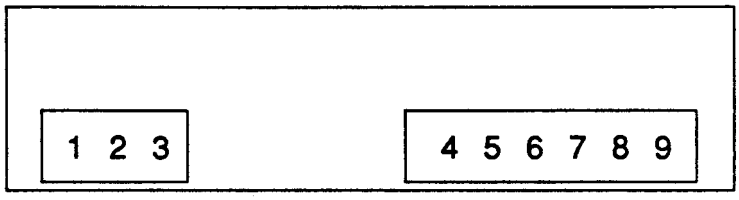
Output load regulation and cross regulation

+5 V output	± 50 mV
+12 V output	- 600 mV/+2.2 V
-12 V output	± 600 mV
-5 V output	± 250 mV

The above are measured under worse case permutation of loading between minimum and maximum loads.

Signal cable pin assignments

Pin	Function
1	AC live
2	AC neutral
3	Earth
4	+5Vdc
5	Common
6	Common
7	+12 V dc
8	-12 V dc
9	-5 V dc



Pin allocations

13:5 Environmental

Under the following conditions, no damage will occur to the unit:

Temperature (ambient)		
	Operational	0 to 40 deg C
	Non-Operational	-40 to 85 deg C
Relative Humidity		
	Operational	10% to 95% R.H. non-condensing
	Non-Operational	10% to 95% R.H. non-condensing
Mechanical Shock		
	Non-operational	50g on any axis, half sine wave, 10 millisecond duration
Altitude		
	Operational	2500 metres above sea level

13.6 Reliability and data integrity

Mean time before failure: 50,000 hours minimum at 25 degrees centigrade. 80% loading.

13:7 Mechanical dimensions

Height	60 mm
Width	215 mm
Depth	117.5 mm
Weight	1.25 kgs maximum

13:8 Service and support

Arrangements for service and the supply of service manuals are to be made in accordance with the Acorn Computers 'Support and Service Strategy'.

Chapter 14 Floppy disc drive

14.1 Introduction

This chapter gives the specification details for the 3.5 inch, 2 Mbyte floppy disc drive fitted inside the Acorn Technical Publishing System.

14.2 Safety and EMI requirements

The drive complies with the definition of SELV.

The equipment is designed and manufactured to comply with BS6527, Class B, but not necessarily approved.

Electromagnetic (interference) susceptibility

The following are the limits of electrical interference which may be present without causing the equipment to:

- deviate from its specification, ie give soft errors
- become damaged such that repairs or replacement of components are required, ie cause physical damage.

	Office Use
Electrostatic Discharge:	
Lower level - shall not cause malfunction (soft errors)	6 kV
Upper level - shall not cause physical damage, but visible malfunction is permitted.	12 kV

14.3 Specification

The disc drive has a 1 inch high Acorn grey bezel and button. The disc eject button is located on the right hand side of the front bezel. An amber LED is situated in the bottom left hand corner of the front bezel.

- Disc size: 3.5 inch
- Capacity: 2 Mbytes (unformatted MFM)
- Heads: 2
- Cylinders: 80
- Operates without write precompensation
- Serial data rate: 250 kbit/second with 1 Mbyte media using MFM encoding and 500 kbit/second with 2 Mbyte media using MFM encoding
- Track to track step rate: 3 ms
- Seek settle time: 15 ms maximum
- Average seek including head settling time: 30 ms maximum
- Write to read timing: 1200 µs maximum
- Power-on to drive ready: 1000 ms maximum
- Power requirements +5 V rail only, better than ±10%, 2 W maximum continuous
- Capable of reading 1 Mbyte Acorn disc format and reading/writing 2 Mbyte Acorn disc format

Signal cable pin assignments

Pin	Function	Pin	Function
1	0V	2	High density select
3	0V	4	No connection
5	0V	6	Drive select 3
7	0V	8	Index
9	0V	10	Drive select 0
11	0V	12	Drive select 1
13	0V	14	Drive select 2
15	0V	16	Motor on
17	0V	18	Direction
19	0V	20	Step/disc change reset
21	0V	22	Write data
23	0V	24	Write gate
25	0V	26	Track 0
27	0V	28	Write protect
29	0V	30	Read data
31	0V	32	Side 1 select
33	0V	34	Disc changed

LED is on when select signal is active low.

Signal connector: 34 way connector, 2 row, male, 0.1 inch pitch.

Input and output levels

Input and output levels must be TTL compatible. Interface lines are pulled up with 1 kOhm pull up resistors.

14:4 Power supply

Supply rail: +5 V dc
Tolerance: ± 10 %

Acceptable supply noise: 100 mV peak to peak
Bandwidth noise measured: 0-30 MHz
Maximum power continuous: 2 Watts

Power connections

Pin	Function
1	+5 V
2	ground (+5 V return)
3	ground
4	no connection

Power connector: 4 pin, 2.5 mm pitch, right-angled, PCB mounting.

14.5 Environmental

Under the following conditions, no damage will occur to the drive:

Temperature (ambient)
Operational 10 to 50 deg C Non-Operational -20 to 50 deg C

Relative Humidity
Operational 20% to 80% R.H. non-condensing
Non-Operational 5 to 95% R.H. non-condensing

Mechanical Shock
Operational 5g maximum x 10 ms, half sine wave Non-operational 60g maximum x 10 ms, half sine wave

Vibration
Operational 0.5g peak, 20-500 Hz sine wave
Non-operational

Mounting angle: -5 to +30 degrees from the horizontal plane

14:6 Reliability and data integrity

Mean time before failure: 12,000 power-on hours minimum

Media life greater than 3 X 10^6 revs per track

Diskette insertions greater than 30,000

Design life greater than five years

Soft errors: Less than 1 in 10^9 bits reading
Hard errors: Less than 1 in 10^{12} bits reading
Seek errors: Less than 1 in 10^6 seeks

14:7 Mechanical dimensions

Bezel height: 25.4 ± 0.2mm (relative to mounting holes, ± 0.5mm)
Bezel width: 101.6 + 0-0.4 mm
Bezel rear to front mounting holes: 21.0 ± 0.3mm (side)
Front mounting holes to middle holes: 60 ± 0.2 mm
Front mounting holes to rear holes: 90 ± 0.2 mm
Bezel bottom to side mounting holes: 5.0 ± 0.3 mm
Holes threaded M3, depth 4 mm

14:8 Service and support

Arrangements for service and the supply of service manuals are to be made in accordance with the Acorn Computers 'Support and Service Strategy'.

Chapter 15 Cartridge tape drive

15.1 Introduction

This chapter gives the specification detail for the 3.5 inch, 40 Mbyte cartridge tape drive which is fitted internally to the Acorn Technical Publishing System.

The bezel is black, and there is an amber LED located in the top right hand corner.

15:2 Specification

- Formatted capacity: 40 Mbytes
- Hardware interface: standard floppy interface - SA475/450
- Hardware interface signal levels: TTL
- Removable terminator resistors fitted (150 S2)
- Firmware interface: produces 20 track format tape with inter-sector servo bursts controlling read/write head positioning. Interprets commands inputted via step line.
- Tape format: format 44
- Data transfer rate: 500 Kbits per second
- Tape speed 50 ips when performing read/write operations
- Tape speed 70 ips when performing fast rewind/erase operations
- Speed variation instantaneous: ± 3.5%
- Speed variation long term: ± 3.5%
- Operates with write precompensation of ± 125 nanoseconds
- Data encoding method is MFM

Signal cable pin assignments

Pin	Function	
2	Pulled to +5 V via 150 Ohms	I/P
4	No connection	
6	Drive select 4	I/P
8	Index	O/P
10	Drive select 1	I/P
12	Drive select 2	I/P
14	Drive select 3	I/P
16	Pulled to +5 V via 150 Ohms	I/P
18	Pulled to +5 V via 150 S2	I/P
20	Step	1/P
22	Write data	I/P
24	Write gate	I/P
26	Busy/track 0	O/P
28	Write protect	O/P
30	Read data	O/P
32	Pulled to +5 V via 150 Ohms	I/P
34	No connection	O/P

Pins: 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31 and 33 are all at 0 V.

15:3 Environmental

Under the following conditions, no damage will occur to the drive and no data will become unreadable.

Temperature (ambient)		
	Operational	5 to 45 deg C
	Non-operational	-30 to 60 deg C
Relative humidity range		
	Operational	20% to 80% RH non-condensing
	Non-operational	5% to 95% RH non-condensing
Altitude		
	Operational	up to 3,000 metres above sea level
	Non-operational	up to 6,000 metres above sea level
Vibration (three axis)		
	Operational	1.0g at 5 to 1000 Hz
	Non-operational	5.0g at 5 to 1000 Hz
Shock (three axis)		
	Operational	5.0g x 11 milliseconds, 1/2 sine wave pulse
	Non-operational	60g x 11 milliseconds, 1/2 sine wave pulse

15:4 Power supply

Supply rail:	+5 V dc	+12 V dc
Tolerance:	± 5%	± 5%
Current:	0.9 A	1.2 A
Current surge:		1.8 A x 400 milliseconds

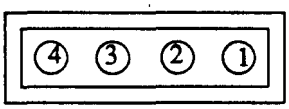
Noise: 100 mV peak to peak

Bandwidth noise measured: 0-30 MHz

Power dissipation: 19 W

Power connections

Pin	Function
1	+12 V
2	ground (+12 V return)
3	ground (+5 V return)
4	+5 V



Pin allocations

Power connector 4 pin, 2.5 mm pitch, right-angled, PCB mounting, Acorn part number 0800,506.

15.5 Reliability and data integrity

Mean time before failure: greater than 50,000 hours excluding head wearout.

Head life: 2,000 hours minimum of tape motion.

15.6 Mechanical dimensions

Height	1.705 inches
Width:	4.090 inches
Depth:	5.81 inches

15.7 Service and support

Arrangements for service and the supply of service manuals are to be made in accordance with the Acorn Computers 'Support and Service Strategy'.

Chapter 16 Internal hard disc drive

16.1 Introduction

This chapter gives the specification detail for the 3.5 inch, 70 Mbyte hard disc drive which is fitted internally to the Acorn Technical Publishing System :

16.2 Safety and EMI

The drive complies with the definition of SELV.

The equipment is designed and manufactured to comply with BS 6527, Class B, but not necessarily approved.

Electromagnetic (interference) susceptibility

The following are the limits of electrical interference which may be present without causing the equipment to:

- Deviate from its specification, ie give soft errors
- Become damaged such that repairs or replacement of components are required, ie cause physical damage.

	Office Use
Electrostatic Discharge:	
Lower level - shall not cause malfunction (soft errors)	6 kV
Upper level - shall not cause physical damage, but visible malfunction is permitted.	12 kV

16:3 Specification

- Formatted capacity: 70 Mbytes
- 3.5 inch disc drive
- Interface: SCSI to ANSI X3.131 (controller embedded on drive)
- Firmware complies with ANSI X3.131, Common Command Set Revision 4.0A, reselection supported
- Average seek time is less than 30 ms from command issue to command complete
- SCSI transfer rate of greater than 0.8 Mbytes/second.

Signal cable pin assignments

Pin	Function	Pin	Function
1	0V	2	Data bus bit 0 (LSB)
3	0V	4	Data bus bit 1
5	0V	6	Data bus bit 2
7	0V	8	Data bus bit 3
9	0V	10	Data bus bit 4
11	0V	12	Data bus bit 5
13	0V	14	Data bus bit 6
15	0V	16	Data bus bit 7 (MSB)
17	0V	18	Data bus parity
19	0V	20	Ground
21	0V	22	Ground
23	0V	24	Ground
25	n/c	26	Terminator power (+5 V)
27	0V	28	Ground
29	0V	30	Ground
31	0V	32	Attention
33	0V	34	Ground
35	0V	36	Busy
37	0V	38	Acknowledge
39	0V	40	Reset
41	0V	42	Message
43	0V	44	Select
45	0V	46	Control/Data
47	0V	48	Request
49	0V	50	Input/Output

SCSI interface connector: 50 way, 2 row, 0.1 inch pitch.

16.4 Power supply

Supply rail:	+5 V dc	+12 V dc
Tolerance:	± 5%	± 5%
Current:	< 1.0 A	< 1.2 A
Current surge:		2.5 A max

Acceptable supply noise:

Bandwidth 0-500 Hz	100 mV peak to peak
Bandwidth 500 Hz - 25 MHz	50 mV peak to peak

Bandwidth noise measured: 0-30 MHz

Power dissipation: 10 W

Terminating resistors fitted.

Power connections

Pin	Function
1	+12 V
2	ground (+12 V return)
3	ground (+5 V return)
4	+5 V

Power connector: 4 way connector (Acorn part number 0800,506)

16.5 Environmental

Under the following conditions, no damage will occur to the hard disc drive and no data will become unreadable.

Temperature (ambient)	
Operational	10 to 50 deg C
Non-operational	-30 to 60 deg C
Thermal shock	
Operational	maximum rate of change 20 deg C/hour
Non-operational	rate of change which causes no condensation
Relative humidity range	
Operational	10% to 80% RH non-condensing
Non-operational	8% to 90% RH non-condensing
Altitude	
Operational	up to 2000 metres above sea level
Non-operational	up to 10,000 metres above sea level
Vibration	
Operational	0.5g peak, 5-500 Hz, sine wave
Non-operational	1.0g peak, 5-500 Hz, sine wave
Shock	
Operational	6g maximum x 10 ms, half sine wave
Non-operational	40g maximum x 10 ms, half sine wave

16:6 Reliability and data integrity

Mean time before failure: greater than 20,000 hours (power on)

Recoverable read error:	less than 1 in 10^{10} bits
Non-recoverable read error	less than 1 in 1^{12} bits
Seek errors:	less than 1 per 1^{6} seeks

16.7 Mechanical dimensions

Height	1.625 inches
Width	4.00 inches
Depth	5.75 inches

16.8 Service and support

Arrangements for service and the supply of service manuals are to be made in accordance with the Acorn Computers 'Support and Service Strategy'.

Chapter 17 Monochrome monitor

17.1 Introduction

This chapter details the specification of the monochrome monitor which is delivered as part of the Acorn Technical Publishing System to provide high resolution graphics capabilities. The monitor has a tilt and swivel base to allow positioning for easy viewing.

17.2 Safety and EMI standard

The monitor is designed to comply with the following standards:

Safety
BS5850 (IEC 380)
IEC950
UL478 (5th addition)
CSA 22.2 220
BS415 (IEC65)

Electromagnetic emission
BS6527 Class A
VDE 0871 Class A
FCC Regs. Part 15, sub part J (Class A).

17.3 Specification

- Size: 19 inches
- Screen area: 340 mm horizontal x 255 mm vertical
- Aspect ratio: 4 to 3
- Resolution: 1168 pixels by 904 rows
- Horizontal: 1152 plus border of 16 pixels equally divided both sides of the display
- Vertical: 900 plus border of four rows equally divided above and below the active display
- Phosphor type: medium-short persistence, paper white
- Faceplate treatment Antiglare direct etch or coating with light reflective factor of lower than 60%

Geometric and linearity distortion

Geometry: The edge of the active video falls within the boundaries of two concentric ideal rectangles separated by 4 mm.

Linearity: Horizontal and vertical linearity is defined as the difference in height or width between cells in a cross hatch pattern. This pattern covers the whole of the active display, and has a cell size of at least 1 inch. The difference in size of any two adjacent cells must be less than 6%, and the greatest difference in size between any two cells in the active display must be less than 10%.

Horizontal timings

Pixel dot rate: 96.0000 MHz

	Pixels	Duration		
		min	nom	max
Sync Width:	208 (nom)	1.5µs	2.166 µs	2.3 µs
Back Porch:	188 (nom)	1.0 µs	1.958 µs	2.7 µs
Sync plus Back Porch:	396 (nom)	4.0 µs	4.125µs	4.2 µs
Border #1	8 }			
Active Display:	1152 }	12.167 µs		
Border #2:	8 }			
Front Porch:	4	0.042 µs		

TOTAL 1568 Pixels

Horizontal frequency: 61.224 kHz ± 1%

Vertical timings

	Lines	Duration
Sync Width:	3	49 µs
Back Porch:	43	702 µs
Top Border:	2	
Active Lines:	900	14.77 ms
Bottom Border:	2	
Front Porch:	0	0 µs

TOTAL 950 Lines

Refresh rate: 64.4 frames/second non interlaced

Bandwidth: 100 MHz.

17.4 Input signals

Video signal:	Analogue
Amplitude:	0 to 0.7 volts
Impedance:	75
Signal polarity:	Positive going
Composite sync:	TTL
Sync polarity:	Negative going pulse triggered off the leading (ie falling) edge.

17.5 Mains power input

The monitor is rated for the following AC mains input ranges. Selection is automatic or via external manual selector device:

	MIN	NOM	MAX	UNITS
United Kingdom				
Operating Voltage Range	216	240	264	VAC
Line Frequency	47	50	53	Hz
Europe				
Operating Voltage range	198	220	242	VAC
Line Frequency	47	50	53	Hz
USA/Canada				
Operating Voltage range	98	110	132	VAC
Line Frequency	56	60	63	Hz

Power consumption is less than 200 Watts.

17.6 Connectors and leads

Mains AC inlet to the monitor is an IEC 3 pin male.

Signal connectors are BNCs, one for sync and one for video.

17.7 Additional components

A power lead is required to connect from the power outlet of the main workstation to the input of the monitor. The lead has an IEC 3 pin female at one end and an IEC male at the other.

Length: 1.5 metres, Acorn part number 0870,355

Two BNC to BNC, 75 Ohm coaxial cables are required to interconnect between the BNC connectors on the monitor and corresponding BNC connectors on the Acorn Technical Publishing System.

Length: 1.5 metres, Acorn part number 0870,706

17.8 Controls and Indicators

The following controls are available:

- mains ON/OFF switch
- brightness control
- contrast control.

The ON/OFF indicator is green.

17:9 Environment

The following specification applies to the unit of which the monitor is a part.

Temperature (ambient)	
Operational	10C to 35 C
Non-operational	-30 to + 60, degrees C ambient free air temperature
Thermal shock	
Non-operational	+60 C to -30 C, repeated three times to Acorn standard 0980,530.
Relative humidity range	
Operational	10% to 80% RH, non-condensing
Non-operational	5% to 95% RH, non condensing
Altitude	
Operational	-300 metres to 2500 metres above sea level
Non-operational	10,000 metres above sea level
Vibration	
Non-operational	Random vibration to BS2011, part 2.1, test Fd with the following parameters: 20-2000 Hz, 0.005 g2/Hz. Two hours in each plane, six hours total.
Shipment and storage	Random vibration to BS2011, Pt 2.1 Test Fd with the following parameters 20-2000 Hz, 0. 005 g2/Hz, decreasing linearly to 0.001 g2/Hz at 2000 Hz, 6 hours total, 2 hours in each perpendicular plane.
Mechanical shock	
Non-operational	Being tilted about each of the bottom edges to a height of 100mm or 30 degrees to the horizontal, (whichever is the most severe) and then dropped three times from each corner. Three parallel falls from a height of 100mm. Three impacts of 0.5N on each accessible face.

17.10 Reliability

The unit has a mean time to failure (MTBF) of 20,000 hours minimum at a ground fixed environment 25 degrees centigrade ambient calculated according to MIL-HDBK-217D.

17.11 Service and support

Arrangements for service and the supply of service manuals are to be made in accordance with the Acorn Computers 'Support and Service Strategy'.

Chapter 18 External storage unit

18.1 Introduction

The external storage system can be attached to the Acorn Technical Publishing System to provide the user with high speed secondary mass data storage facilities.

It consists of:

- the external storage unit (see the description below)
- a screened SCSI interface cable
- a mains cable
- a blank DC600A cartridge (streaming tape version only).

18.2 External storage unit

The external storage box contains a switched mode power supply and one of the following:

- 150 MByte 5.25 inch half height format (1.75 inches) cartridge streaming tape drive mechanism, Acorn part number 0912,001.
- 280 MByte 5.25 inch full height format Winchester disc drive, Acorn part number 0912,002.

The storage box allows additional SCSI devices to be daisy chained onto the SCSI bus.

See also Chapter 19, *Streaming tape drive* and Chapter 20, *External hard disc drive* for details of each of the above components.

18.3 Safety and EMI

The equipment is designed and manufactured to comply with the following standards:

Electrical safety
IEC 380
CEE 22

Interference generation
VDE 0871 class A

18.4 Specification

See Chapter 19, *Streaming cartridge tape* and Chapter 20, *External hard disc drive* for the specification of each type of storage unit.

18:5 Inter-connections

SCSI cable
Via a fully-shielded round 50-way IDC cableform, whose screen is grounded at each end. The cable is terminated at each end with a 50-way delta (Centronics-type) male plug. The length is 1.2 metres, Acorn *part* number 0174,790.

A 0.4 metre cable is available as an optional extra - Acorn part number 0174,734.

Mains cable
The mains cable is two metres long IEC fitted with moulded 13 Amp plug (UK version) or moulded SCHUCO plug (European version).

A one metre long IEC male to IEC female jumper cable, Acorn part number 0870,355, is available as an option.

SCSI Interface

SCSI single ended interface, as defined in ANSI X131. The last unit in the SCSI 'chain' is fitted with a 330/220 Ohm line terminator plug. This is supplied with the Acorn Technical Publishing System main computer unit. The SCSI sockets are electrically identical, and connections may be made to either.

18:6 Controls and indicators

The following controls are available:

Controls

- double-pole mains circuit breaker on front panel
- cartridge lock/eject slide lever (on versions fitted with a streaming tape drive)

Indicators

- mains ON/OFF switch (green LED)
- cartridge tape loaded (amber LED) (streaming tape version only)
- Winchester drive access (amber LED) (hard disc version only).

18:7 Connectors

Power inlet
3 pin IEC fused plug. 2 A T 20x5mm D LBC fuse.

Power outlet
3 pin IEC unfused, unswitched socket. 6 A maximum current.

SCSI connector
2 x 50 way delta (centronics type) female, panel mounted RFI screened. These are identical.

SCSI
The 50-way interface cable signal names and pin numbers are detailed below:

Pin number	Mnemonic	Description
2	*DB0	Data bus bit 0
4	*DB1	Data bus bit 1
6	*DB2	Data bus bit 2
8	*DB3	Data bus bit 3
10	*DB4	Data bus bit 4
12	*DB5	Data bus bit 5
14	*DB6	Data bus bit 6
16	*DB7	Data bus bit 7
18	*DBP	Data bus parity (odd)
20	GND	Ground
22	GND	Ground
24	GND	Ground
26	VCC	Optional Vcc
28	GND	Ground
30	GND	Ground
32	*ATN	Attention
34	GND	Ground
36	*BSY	Busy
38	*ACK	Acknowledge
40	*RST	Reset
42	*MSG	Message
44	*SEL	Select
46	*C/D	Control/data
48	*REQ	Request
50	*I/0	Input/output

All odd pins are signal returns and are connected to signal ground at the device, except for pin 25 which is left disconnected.

18.8 Device ID

As shipped, the drives are configured with the following SCSI device IDs:

Cartridge tape drive unit	5
Winchester drive unit	1

Consult your supplier if you need to change the device ID.

18.9 Mains supply ti on

Up to six external storage units may be daisy chained together by connecting the mains outlet from one unit to the mains inlet of the next unit in the chain using a suitable cable (eg: Acorn part number 0870,355). The computer MUST NOT be connected to this chain, but connected separately to the mains supply.

18.1 Environmental

The equipment is intended to operate under the following environmental conditions:

Temperature (ambient)		
	Operational	5 to 35 deg C
	Non-operational	-30 to 60 deg C
Thermal shock		
	Operational	maximum rate of change 10 deg C per hour
	Non-operational	+60 deg C to -30 deg C repeated three times, to Acorn Procedure 0980, 530.
Relative humidity range		
	Operational	10% to 95% RH non-condensing
	Non-operational	5% to 95% RH non-condensing
Altitude		
	Operational	-300 to 2500 metres above sea level
	Non-operational	Shipping: -300 to 10000 metres above sea level Storage: -300 to 3000 metres above sea level
Vibration		
	Non-operational	0.02 Gsq/Hz from 10 to 60 Hz, decreasing linearly to 0.001 Gsq/Hz from 60 to 500 Hz for one hour in each of the three perpendicular axes.
Mechanical Shock		
	Shipment and storage	Drop test from a height of one metre onto each face and onto any two edges or corners.
Maximum stack height (storage)		1.5 metres

18.11 Reliability

- Operational lifetime: 10,000 hours
- Theoretical mean time between failures: 4,333 hours.

18:12 Maintenance

The tape head should be cleaned according to Acorn's service procedure (tape drive only).

The fan filter should be replaced every three months, or as required by the environment.

18.13 Service and support

Arrangements for service and the supply of service manuals are to be made in accordance with the Acorn Computers 'Support and Service Strategy'.

Chapter 19 Streaming cartridge tape

19.1 Introduction

This chapter gives the specification detail for the 5.25 inch, 120 Mbyte streaming cartridge tape drive which can be fitted internally to the Acorn Technical Publishing System external storage system. The drive complies with the definition of SELV.

See also Chapter 18, *External storage unit.*

19.2 Safety and EMI

The equipment is designed and manufactured to comply with BS 6527, Class B, but not necessarily approved.

Electromagnetic (interference) susceptibility

The following are the limits of electrical interference which may be present without causing the equipment to:

- deviate from its specification, ie give soft errors
- become damaged such that repairs or replacement of components are required, ie cause physical damage.

	Office Use
Electrostatic Discharge:	
Lower level - shall not cause malfunction (soft errors)	6 kV
Upper level - shall not cause physical damage, but visible malfunction *is* permitted.	12 kV

19.3 Specification

The front bezel is black. There is an amber drive active LED on the right side of the unit.

- Formatted capacity: 150 Mbytes
- Drive size: 5.25 inch, half height
- Suitable media: DC 600 A cartridges
- Interface: SCSI to ANSI X3.131 (controller embedded on drive)
- Software complies with ANSI X3.131, Common Command Set Revision 4.0B
- Reselection is supported
- Tape speed: 90 ips
- Tape recording format: QIC 120
- Read compatibility with tapes recorded in QIC 24 format
- RAM buffer size: 64 kbytes
- Burst transfer rate: 1.25 Mbytes per second maximum

19:4 Power supply

Supply rail:	+5 V dc	+12 V dc
Tolerance:	± 5%	10%
Current:	< 1.0 A	< 1.5 A
Current surge:	-------	2.5 A for 300 ms

Note: Tolerance includes maximum ripple of 100 mV Power

dissipation: 20 Watts typical, 35 Watts maximum.

Terminating resistors are not fitted.

Power connections

Pin	Function
1	+12 V
2	ground (+12 V return)
3	ground (+5 V return)
4	+5 V

Power connector: 4 way connector (Acorn part number 0800,506)

19:5 Environmental

See Chapter 18, *External storage unit.*

19.6 Reliability and data integrity

Mean time before failure: greater than 15,000 hours (power on).

Recoverable read error:	less than 1 in 10^8 bits
Non-recoverable read error	less than 1 in $_{112}$ bits

19:7 Mechanical dimensions

Height	1.625 inches
Width	5.75 inches
Depth	8.00 inches

19.8 Service and support

Arrangements for service and the supply of service manuals are to be made in accordance with the Acorn Computers 'Support and Service Strategy'.

Chapter 20 External hard disc drive

20.1 Introduction

This chapter gives the specification detail for the 5.25 inch, 280 Mbyte hard disc drive which can be fitted internally to the Acorn Technical Publishing System external storage system.

See also Chapter 18, *External storage unit.*

20.2 Safety and EMI

The drive complies with the definition of SELV.

The equipment is designed and manufactured to comply with BS 6527, Class B, but not necessarily approved.

Electromagnetic (Interference) susceptibility

The following are the limits of electrical interference which may be present without causing the equipment to:

- deviate from its specification, ie give soft errors
- become damaged such that repairs or replacement of components are required, ie cause physical damage.

	Office Use
Electrostatic Discharge:	
Lower level - shall not cause malfunction (soft errors)	6 kV
Upper level - shall not cause physical damage, but visible malfunction is permitted.	12 kV

The front bezel of the hard disk drive is black. There is an amber drive active LED mounted on the bezel.

20.3 Specification

- Formatted capacity: nominally 280 Mbytes
- Form factor: 5.25 inch, full height drive
- Interface: SCSI to ANSI X3.131 (controller embedded on drive)
- Firmware complies with ANSI X3.131, Common Command Set Revision 4.0B
- Reselection is supported
- Average seek time: less than 18 ms from command issue to command complete
- Data transfer rate: 1.2 Mbytes/second

20.4 Power supply

Supply rail:	+5 V dc	+12 V dc
Tolerance:	± 5%	± 5%
Current:	< 2.0 A	< 2.0 A
Current surge:	-------	4.3 A for 10 seconds maximum

Acceptable supply noise:

Bandwidth 0-10 MHz	100 mV peak-to-peak

Typical power dissipation: 35 Watts

Note: The tolerance includes a maximum ripple of 100 mV.

Terminating resistors are not fitted.

Power connections

Pin	Function
1	+12 V
2	ground (+12 V return)
3	ground (+5 V return)
4	+5 V

Power connector: 4 way connector (Acorn part number 0800,506).

20.5 Environmental

See Chapter 18, *External storage unit.*

20.6 Reliability and data integrity

Mean time before failure: greater than 20,000 hours (power on)

Recoverable read error:	less than 1 in 10^8 bits
Non-recoverable read error	less than 1 in 1^{12} bits

20.7 Mechanical dimensions

Height	3.23 inches
Width	5.75 inches
Depth	8.00 inches

20.8 Service and support

Arrangements for service and the supply of service manuals are to be made in accordance with the Acorn Computers 'Support and Service Strategy'.

Chapter 21 Ethernet podule

21.1 Introduction

This chapter describes the hardware design and architecture of the Ethernet podule. This product provides users of the Acorn Technical Publishing System with a high performance network capability designed to conform to the IEEE 802.3 10base5 (Ethernet) and 10base2 (Cheapernet), 10 Mbps baseband standards.

Ethernet was developed by the Xerox Corporation in the early 1970s and a specification made available in 1980. This specification known *as the* 'Blue Book' was used as the basis for the IEEE and ECMA standards. AU new equipment (including this product) is or should be designed to the IEEE standard. This allows interworking with existing Ethernet equipment, at least at the physical level.

The remainder of this document makes the following assumptions about the reader:

- A working knowledge of the Acorn podule bus is assumed. A guide to the Acorn podule bus is in Chapter 10, *Podules and backplane*.
- An understanding of the basic architecture of the Ethernet/IEEE 802.3 standard is assumed. The Intel publication *The LAN Components User's Manual* is particularly useful and contains a suitable introduction to local area network standards. It is recommended that the reader obtain a copy as reference to it is made in this document.

21.2 Specification

Acorn document 0373,000/PS is the product specification.

21.3 Basic operation and block diagram

The figure below is a block diagram of the Ethernet/Cheapernet podule.

The main functional blocks are:

- the net controller: Intel 82586 (LANCE)
- the serial interface adaptor. Intel 82501 (SIA)
- transceiver. Intel 82502
- attachment unit interface (AUI) socket (D-type)
- isolation transformers and power supply
- bus buffers and transceivers
- the RAM buffer
- the RAM page register
- a PROM based 'extended' podule ID
- the control register
- the PAL based state machine.

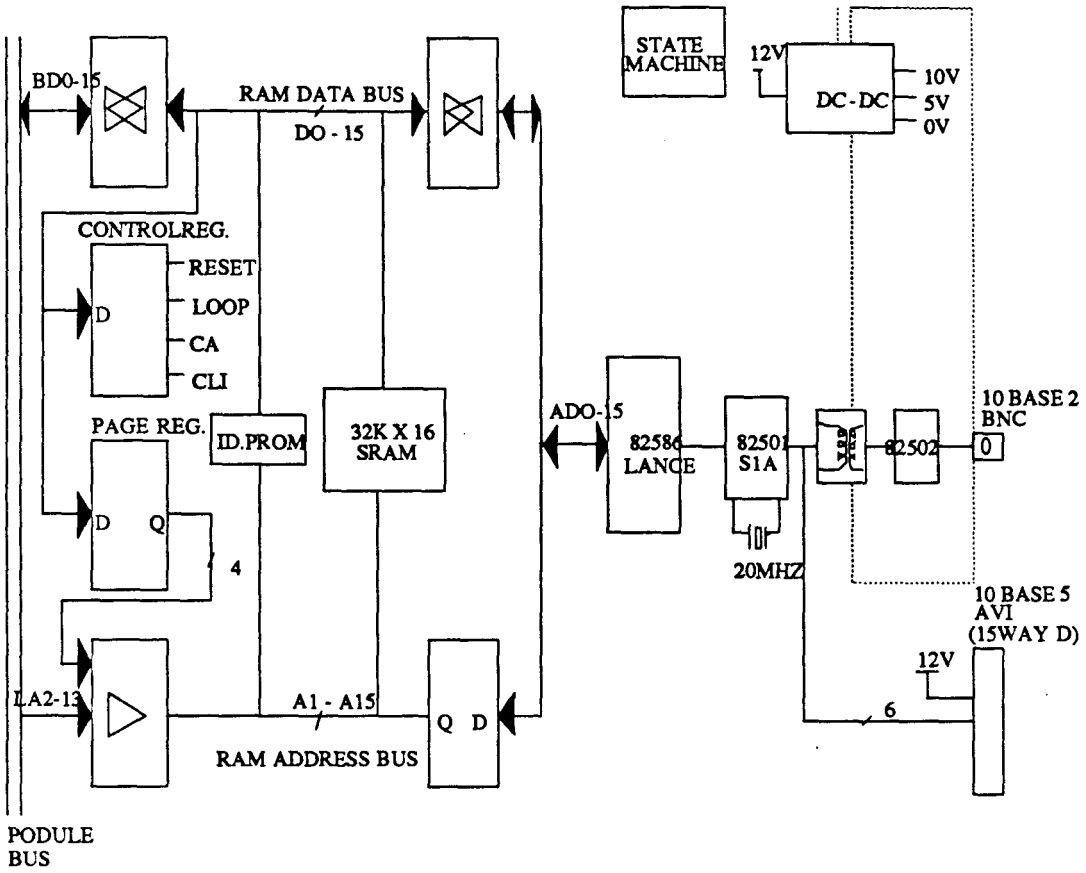


Figure 21.1 : Ethernet podule block diagram

The Intel chip set

As the Xerox and IEEE standards have become widely accepted, a number of systems companies have produced VLSI devices that considerably reduce the design effort required to implement a connection. The most notable of these are by Advanced Micro Devices (AMD) and Intel.

The Intel chip set comprising the 82586 local area network coprocessor, the 82501 ethernet serial interface, and the 82502 ethernet transceiver chip has been used in this design.

The 82586 and other similar local area network controllers are generally referred to by the acronym LANCE, even though this is a trademark of AMD.

The 82586 LANCE performs media access control, framing, pre/postamble generation and stripping, source address generation, CRC checking, and short packet detection. In addition diagnostic functions such as Time Domain Reflectometry (TDR) can be performed.

The 82501 serial interface adapter (SIA) performs Manchester encoding/decoding, receive clock recovery and directly drives the attachment unit interface (AUI) to the cable mounted ethernet transceiver. In addition the 82501 operates a watchdog to prevent continuous transmission (a fault condition), and provides a loop-back test facility. A second source for this device is SEEQ who manufacturer a similar part, the DQ8023A. This part however is not identical and will not perform TDR correctly.

The 82502 transceiver applies transmit data to, and removes receive data from the Cheapernet cable interface. This devices performs a similar function to the cable mounted Ethernet *transceiver.*

The dual port memory

The LANCE is a true coprocessor and is designed to perform scatter-gather DMA. In common with other LANCE chips the 82586 will utilise a significant bus bandwidth when operating on a net running at 10 Mbps (note: this is not simply the serial data rate divided by the parallel bus width). This bandwidth cannot be provided by the ARM processor over the podule bus and so a dual-port memory system has been implemented.

All communication between the ARM and the LANCE is carried out through command blocks in the dual-port RAM (there are no visible registers in the 82586 LANCE). These command blocks and associated data structures are defined and described in Intel's data sheet, listed in Appendix E.

To issue a command to the LANCE the ARM appends the command to the command block list (CBL) in the dual-port RAM. It then raises the channel attention (CA) signal to the LANCE signalling the presence of the new command. The LANCE responds to CA by reading the command from the CBL and executing as required.

The *LAN Components User's Manual* (reference 9 in the Bibliography) contains a considerably more detailed and comprehensive description of the operation of the LANCE. It is recommended that you obtain a copy, as it contains too much information to include here.

Control register

The control register contains four bits:

Reset (RST) Bit 0:
This bit controls the RESET pin on the LANCE. This bit is set (LANCE reset) on system power-up/hard reset or writing to the control register with this bit logic 1. This bit is cleared (and the LANCE released from the reset state) by writing to the control register with this bit logic 0.

Loop-Back (LB) Bit 1
This bit selects the loop-back mode of 82501 SAI chip. This bit is set and the SIA chip put into loop-back mode by the ARM writing to the control register with this bit logic 1. This bit is cleared (SIA taken out of loop-back mode) on system power-up/hard reset or writing to the control register with this bit logic 0.

Channel Attention (CA) Bit 2
This bit generates a correctly timed CA pulse when the ARM writes to the control register with this bit logic 1. No CA pulse is generated if the ARM writes to the control register with this bit logic 0.

Clear Interrupt (CLI) Bit 3
This bit clears the podule interrupt flag and removes the podule interrupt when the ARM writes to the control register with this bit logic 1. The podule interrupt and flag are unaffected if the ARM writes to the control register with this bit logic 0.

Each bit in the control register is not independent and when writing to a particular bit, the remaining three must be valid. The remaining 12 bits are ignored by the hardware (zero is recommended).

Podule Identification PROM

The podule identification PROM contains the following information:

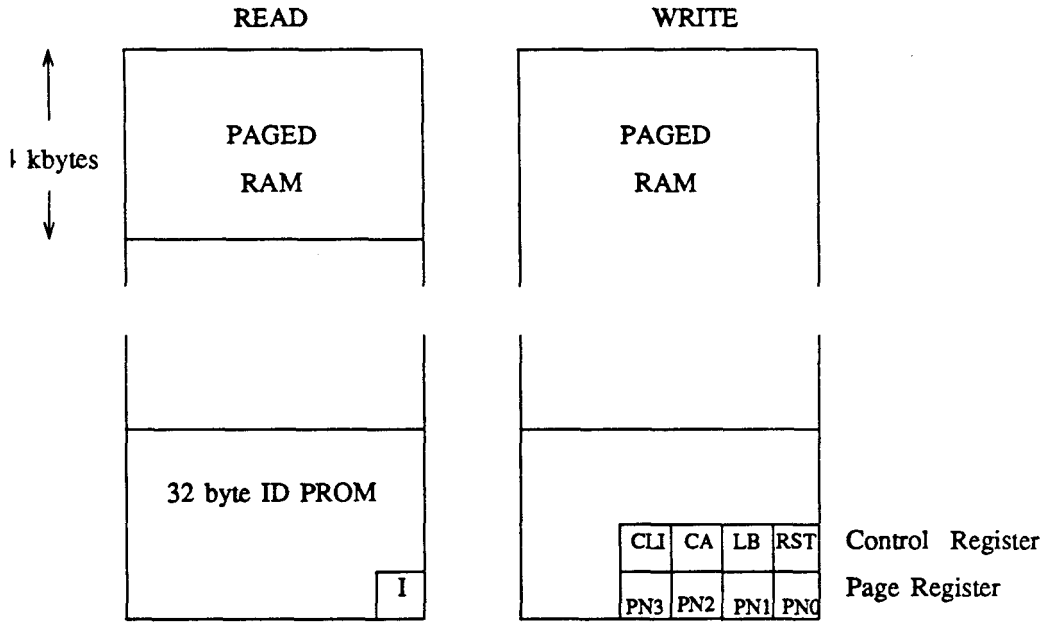
- the Acorn podule identity number (03)
- the interrupt (IRQ) flag bit
- the PCB revision number
- the six byte IEEE globally assigned address block
- a CRC to allow the PROM to be validated.

The contents and operation of the interrupt flag are described in *Interrupts in Detailed description* below.

21.4 Detailed description

Address map

The Ethernet podule address map (offset relative to slot base) is shown in the table below. The RAM buffer occupies the upper half of the podule address space. The ID PROM, page register and control register occupy the lower half.



ID PROM (Base)	= Slot base	(Type 3 access) + 0x0000 (Read only)
Page Register	= Slot base	(Type 2 access) + 0x0000 (Write only)
Control Register	= Slot base	(Type 2 access) + 0x0004 (Write only)
Dual-Port RAM	= Slot base	(Type 2 access) + 0x2000 (Read/write)

Table 21.1: Ethernet podule address map

The LANCE

The 82586 LANCE is a 'scatter-gather' DMA controller type device and is designed to interface to 80186 type processors using a HOLD/HOLDA protocol to resolve arbitration for access to shared memory.

The ARM podule bus cannot easily support a HOLD/HOLDA type interface. This is because the ARM is a dynamic device and cannot be stopped for the required time. (This can be longer than 10 µs during the interframe/interpacket spacing time.) The ARM cannot be given priority and HOLDA deasserted because this will result in the net

controller failing to meet the timing requirements of the net protocol due to the increased bus latency. For example, this could result in the failure of the net controller to take part in the back-off and retry sequence following a collision on a heavily loaded net.

In this design HOLD and HOLDA are wired together and ARM cycles cause wait-states to be inserted into the LANCE bus cycle. This is achieved by removing the READY signal to the LANCE while the ARM is active. Adopting this scheme avoids the problems outlined above. The ARM is never stopped and the LANCE sees minimal bus latency:

The LANCE ARDY/SRDY input used can be programmed to be either asynchronous/ ARDY and internally synchronised, or synchronous/SRDY and externally synchronised. In this *case* it is SRDY mode that must be selected. This is achieved by issuing a configure command with the ARDY/SRDY bit set to logic 1. This is important as the LANCE powers-up in ARDY mode.

In certain circumstances the LANCE needs to perform read-modify-write bus cycles with lockout. Using READY to insert wait-states does not allow this. However lockout is only required when the LANCE updates error counts (statistics) and even then a problem only arises when a count overflows and the ARM resets it to zero while the LANCE is in the modify phase of a read-modify-write cycle. This is solved by the ARM reading back the count after it sets it to zero. If the count is still indicting an overflow then a read modify-write cycle was in progress and the ARM has to correct the count. Error counts this high indicate a major problem that will require correction so should be a rare event.

The memory bus of the LANCE is operated in 'minimum mode' as the timing parameters for LANCE outputs in this mode are subject to less spread between devices. The pull-up resistors on WR*, RD*, and BHE are required to prevent RAM cycles when the LANCE is inactive.

The LANCE communicates directly with the SIA (IC24) via a serial channel comprising seven signals: TXC, TXD, RXC, RXD, RTS, CRS and CDT. The function of each of these is described in the LANCE data sheet. The Clear-to-Send (CTS*) input is not supported by the SIA and is connected to 0 V (enabled).

Dual port RAM

The podule bus provides only a limited space in the address map (8 kbytes) for each podule. This is insufficient and so a paged scheme has been implemented.

Viewed from the ARM side the RAMs are paged into the top half of podule space by a ` page register'. The four bit page register is split across two PALs *(see the* section *The PALs* below). Sixteen pages each of 4 kbytes provide 64 kbytes in total. This is organised as 32 k x 16 bits (two 32 k x 8 static RAMs). An alternative RAM size of 8 k x 16 bits (two 8 k x 8 static RAMs) can be supported (see the section *Links later in* this chapter).

The podule address bus (LA2-13) *is* buffered by two HCT244 (IC66 and IC58) and the podule data bus (BD0-BD15) is buffered by and two HCT245 transceivers (IC15 and IC54). The direction of the data bus transceivers is determined by the podule R/W signal, while both output enables (AAOE and BDOE) are generated by the bus control PAL (IC36).

Viewed from the net controller side, the RAM will be contiguous from location 0x0000 to 0xFFFF. The initialisation root for the controller is 0x0FFFFF6 which is mapped into the RAM at 0xFFF6. The high order address bits are not decoded.

The LANCE address/data bus (AD0-AD15) is demultiplexed by two HCT245 (IC17 and IC22) which use the LANCE ALE signal to latch the address bus. The data bus only requires buffers and two HCT573 transceivers (IC10 and IC32) are used. The direction of the data bus transceivers is determined by the LANCE DT/R signal, while the output enables are generated by the bus control PAL (IC36).

The LANCE is capable of operating on an eight bit bus and is reset to this mode. The LANCE initialisation root (read when released from reset) contains a bit that defines the bus width and this must be set to 0 (=16 bit bus). Until the LANCE reads this it deasserts Byte High Enable (BHE*) and outputs address bits on AD8-AD15 for the entire cycle. To avoid a bus clash BIM* is used to disable the high order data bus transceiver via the bus control PAL (IC36).

Once initialised to a byte wide bus the LANCE only operates on half words (never bytes) so it not necessary to decode the least significant address bit (AD0) to produce separate RAM write strobes for each byte.

Podule Identification PROM

The device used is a 32 byte PROM 27LS19 (IC14).

A typical content of an ID PROM is shown in Table 21.2 below.

The ID PROM shares address and data bus buffers with the RAM. Viewed from the ARM side the ID PROM is byte wide and word aligned.

The podule specification defines two bits in the ID byte to be interrupt flags. This design requires only IRQ interrupts so the FIQ flag is always zero. The IRQ flag is generated by connecting the podule interrupt signal to the most significant address pin. The content of the upper half is similar to the lower half but has the IRQ flag bit set, in this way the interrupt flag is multiplexed 'into' the 1D byte.

Bytes 09 - 0E are the six byte Ethernet address unique across all Ethernet equipment from manufacturers worldwide.

The CRC (Bytes 1C - 1F) *is* calculated on the rest of the PROM (Bytes 00 - 1B) using a 32 bit Autodin - 1I CRC polynomial. This is the same algorithm as the LANCE uses to perform multicast address filtering (see the section *PROM CRC calculation* below). Since each PROM is unique the CRC is used to perform verification.

The output enable is generated by the bus control PAL (IC36).

	D7	D6	D5	D4	D3	D2	D1	D0	NOTES
1F	C	C	C	C	C	C	C	C	CRC on bytes 00 - 1B
1E	C	C	C	C	C	C	C	C	
1D	C	C	C	C	C	C	C	C	
1C	C	C	C	C	C	C	C	C	
1B	Bytes 11 to 1B = 00								
11									
10	0	0	0	0	0	0	0	1	01 - no FIQs, IRQ = 1
0F	0	0	0	0	0	0	0	0	00 - RSVD
0E	I	I	I	I	I	I	I	I	Unique ID
0D	I	I	I	I	I	I	I	I	
0C	I	I	I	I	I	I	I	I	
0B	1	0	1	0	0	1	0	0	A4
0A	0	0	0	0	0	0	0	0	00
09	0	0	0	0	0	0	0	0	00
08	0	0	0	0	0	0	0	1	01 - PCB rev. eg one
07	0	0	0	0	0	0	0	0	00 - UK
06	0	0	0	0	0	0	0	0	Acorn
05	0	0	0	0	0	0	0	0	
04	0	0	0	0	0	0	0	0	Ethernet
03	0	0	0	0	0	0	1	1	
02	0	0	0	0	0	0	0	0	00 - RSVD
01	0	0	0	0	0	0	0	0	00 - no boot code
00	0	0	0	0	0	0	0	0	00 - no FIQs, IRQ = 0

Table 21.2 : Podule identity PROM

The PALS

Three PALs are used in this design:

- the main state PAL (IC29)
- the interrupt and channel attention PAL (IC78)
- the device enable control PAL (IC36).

The main state PAL (IC29)
This PAL implements a state machine which provides timing information for the other two PALS in the design. In addition it produces the two least significant bits of both the page register (PR0 and PM) and control register (RSTO and LOOP).

The interrupt and channel attention PAL (IC78)
This PAL implements the two most significant bits of both the page register (PR2 and PR3) and control register (CLI and CA).

The device enable control PAL (1C36):
This device decodes the address map to provide various device output enables.

The state machine and operation

The state machine has four states; IDLE, SA1, SA2, and SA3 and is clocked from state to state on the falling edge of CLK8, the 8 MHz podule bus clock. The figure below is the state diagram.

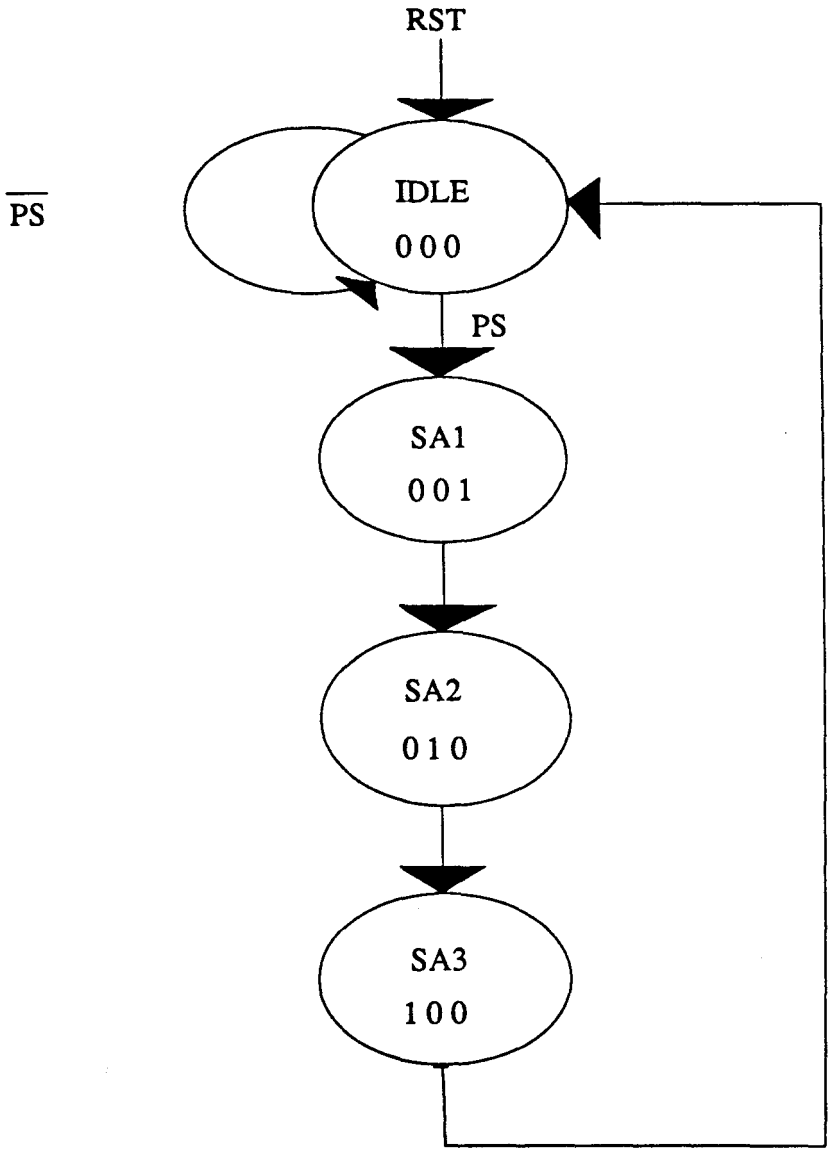


Figure 21:2: State diagram

The idle state
The state machine enters this state on power-up, hard reset (RST* low), or from the SA3 state. In this state the bus buffers on the ARM side of the dual-ported RAM are disabled and those on the LANCE side enabled. Other outputs such *as the* page and control register bits remain unchanged. The state machine remains in the idle state until the ARM starts an access (podule select - PS active).

The SA1 state
This state is entered from the idle state only. In this state the LANCE READY signal is disabled, forcing the LANCE to insert wait states if it is active on the bus. The RAM write strobe (RAMWE*) is disabled to prevent writes while the LANCE side of the dual-port RAM is disabled and the ARM side enabled. The state machine exits to the SA2 state unless a reset occurs.

The SA2 state
This state is entered from the SA1 state only. In this state the ARM access is performed and the corresponding device enables are active eg, if a RAM write is performed then the RAM write strobe (RAMWE*) is active. Similarly if a RAM or ID read is required than the RAM or IDOE is active. Writes to the page register or control bits are also performed during this state. READY is still inactive. The state machine exits to the SA3 state unless a reset occurs.

The SA3 state
This state is entered from the SA2 state only. The RAM write strobe (RAMWE*) is disabled to prevent writes while the LANCE side of the dual-port RAM is enabled and the ARM side disabled. The state machine exits to the idle state where any LANCE access that was in progress is completed.

Podule bus cycles

The podule specification requires all ID PROM access to be made using type 3 (sync) IOC bus cycles. All other accesses to the Ethernet podule must be made using type 2 (fast) IOC cycles.

Figure 21.3 below illustrates a read/write to RAM while the net controller is active. The cycle starts with podule select (PS) active and puts the state machine into the SA1 state on the next clock edge. A description of each state that follows is given above.

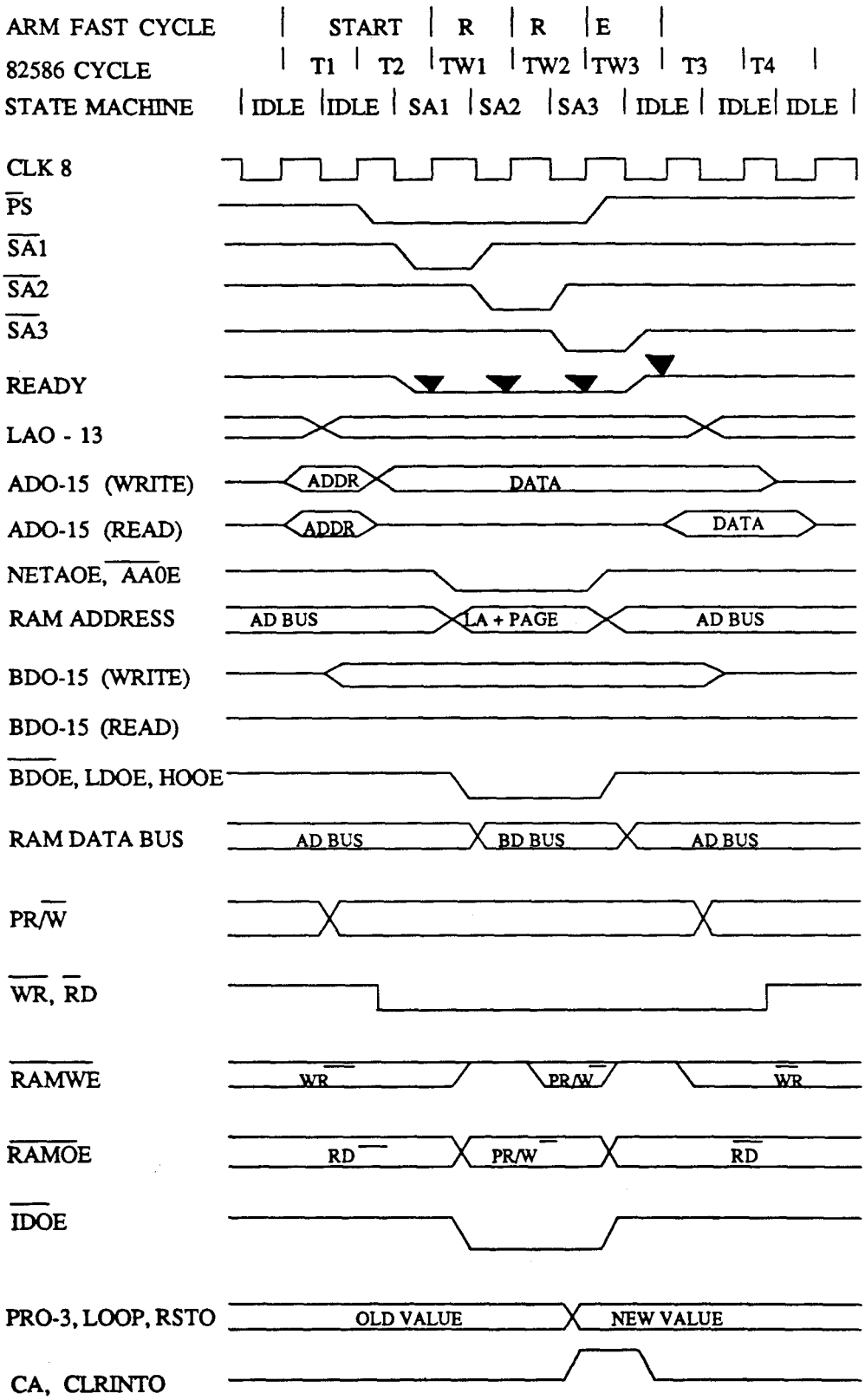


Figure 21.3: Typical podule bus cycle

It should be noted that *Ready* is always deasserted for three cycles, even if the LANCE is idle. A podule bus access can 'collide' with a LANCE access in five different ways, depending on what state the LANCE *is* in when the podule bus access starts. These are: PS* while the lance is in states T1 to T4 **or** idle. The actual number of wait states that the LANCE will insert depends on which of these cases apply. The following four figures illustrate the possible cases.

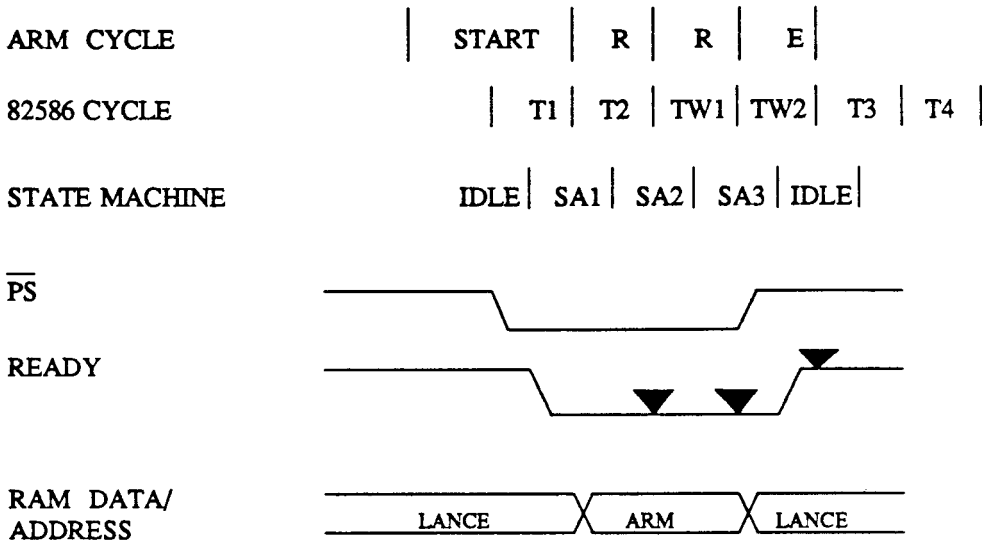


Figure 21.4 : Access collision cases - PS* while LANCE is in T1

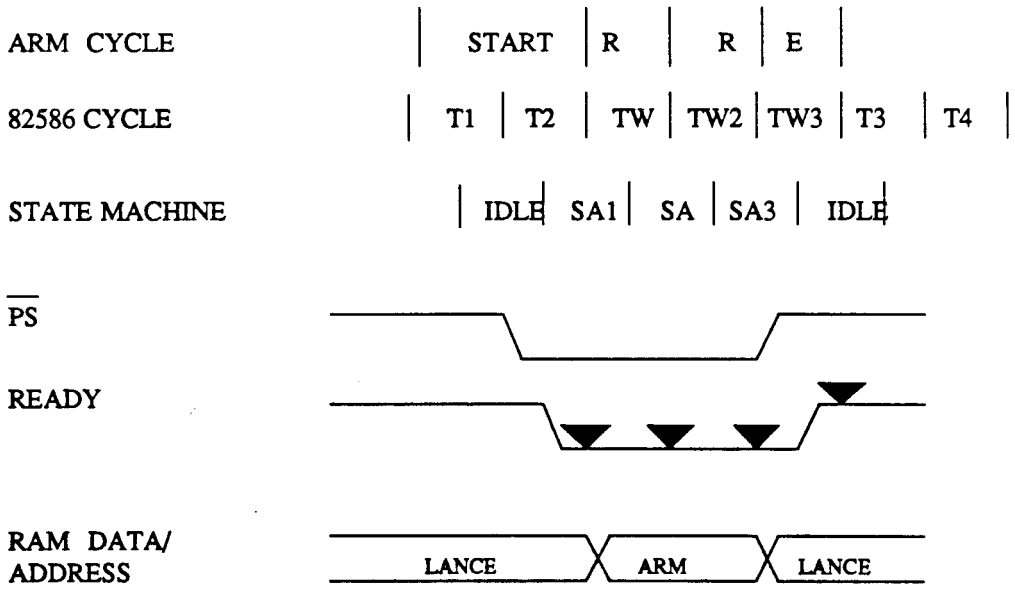


Figure 21.5 : Access collision cases - PS* while LANCE is in T2

PS* while the LANCE is in T1: Figure 21.4:
The LANCE samples READY deasserted at the end of T2 (SA2), and then again at the end of TW1 (SA3), so in this case two wait states are inserted.

PS* while the LANCE is in T.2: Figure 21.5:
The LANCE samples READY deasserted at the end of T2 (SA1), TW I (SA2), TW2 (SA3), so the maximum of three wait states are inserted. Since three wait states is the worst case this is shown in more detail in Figure 21.5.

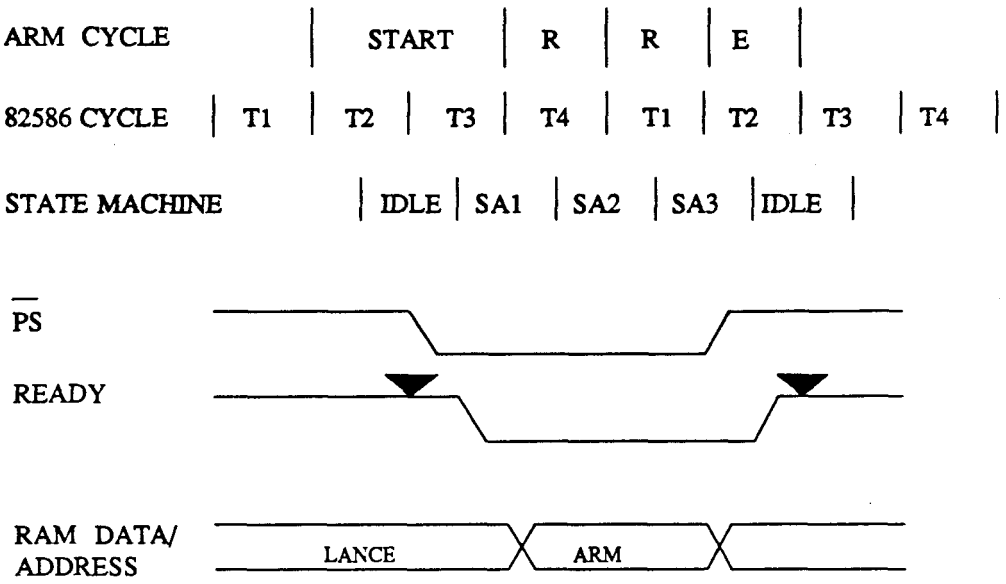
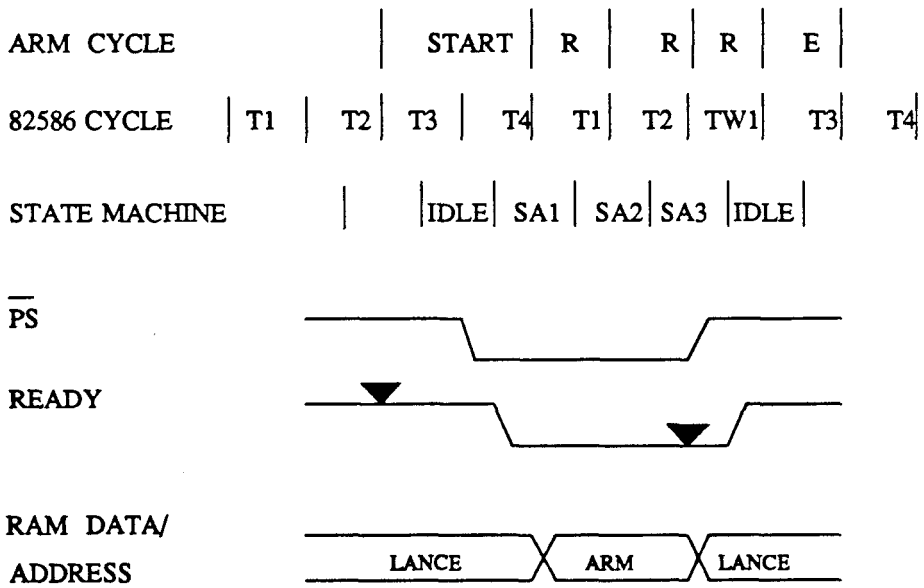


Figure 21.6 : Access collision cases - PS* while LANCE is in T3



PS* while the LANCE is in T3: Figure 21:6:
In this case READY is still active when the LANCE samples it at the end of T3 (idle). This is the last time that the LANCE does this for the current cycle so the LANCE cycle completes before the podule bus cycle starts. Note that the LANCE is not active on the RAM bus during T4.

PS* while the LANCE is in T4: Figure 21:7:
Since the LANCE does not require the bus during T4 no further wait states are inserted in the current cycle. However T1 of the next cycle could follow T4 and one wait state will be inserted into this LANCE access.

PS* while the LANCE is idle.
If the LANCE remains idle while the podule bus cycle occurs then there is no collision and the LANCE ignores the READY signal. This case is not illustrated.

A read from the podule ID PROM or write to the control or page register is similar to a RAM cycle. To simplify the bus design the LANCE is removed from the RAM buses during cycles to these devices.

Bus design note

The cycle stealing scheme should guarantee that the LANCE never has insufficient bus bandwidth or sees excessive bus latency to the extent that it cannot service the net or fails to meet the IEEE timings. Even when the ARM continuously accesses the RAM. The following gives the reasoning behind this statement:

Assumptions:

Net Clock = 10 MHz
Bus Clock = 8 MHz
LANCE FIFO size = 16 bytes

HOLDA is wired to HOLD so:

Bus Latency = 0 cycles

IEEE Interframe Space Time = 9.6 µS
Criteria:

1. FIFO must not over/underrun.

FIFO fill/empty time from serial side:
= 8 (bits) * 16 (bytes) * 100E-9 (bit time)
= 12.8

FIFO empty/fill time from parallel side:
= 8 (Word transfers)
* (4 (standard 8 MHz cycles) + Nwait (wait cycles))
* 125E-9
=4 µs (if Nwait = 0)
=7 µs (if Nwait = 3)
= 8µs (if Nwait = 4)

2. The LANCE must be in a position to transmit by the end of the interframe spacing time.

   With a Fp/Fs ratio of 8 MHz/10 MHz (0.8):
   16*Nwait + Nlatency must be less than or equal to 80.
   If HOLDA = HOLD then Nlatency = 0
   and
   Nwait <= 5

So this strategy works if we can keep the number of wait states (Nwait) less than or equal to five per access. In the current design three are used and this is unlikely to change.

Interrupts

The podule interrupt (PIRQ) is level triggered. However, the interrupt signal (INT) from the LANCE is designed for use with edge triggered interrupt controllers. If the net controller detects a second interrupting condition just after the first is raised, it will drop and reassert INT. The situation could arise where the podule manager (software) may scan the slots and find no IRQ flag set.

The above problem is prevented by latching INT in the interrupt and channel attention PAL (IC78) and using the latched signal INTO to generate the flag. The clear interrupt (CLI) bit in the control register is used to clear the latch.

Latching INT introduces a further problem which is eliminated by a feature of the 82586 LANCE. If a second interrupt occurs after the processor has read the status word in the SCB but before the first is cleared then the second interrupt would be missed. However, if a the interrupt is cleared at the same time as the channel attention (signalling the acknowledge command) is issued, the LANCE will respond by deasserting INT and reasserting if the second interrupt was not acknowledged because it was missed. It is recommended to set CA whenever CLI is set.

Operation of the interrupt latch and the clear interrupt bit is illustrated in Figure 21.8, Figure 21.9 and Figure 21.10 below.

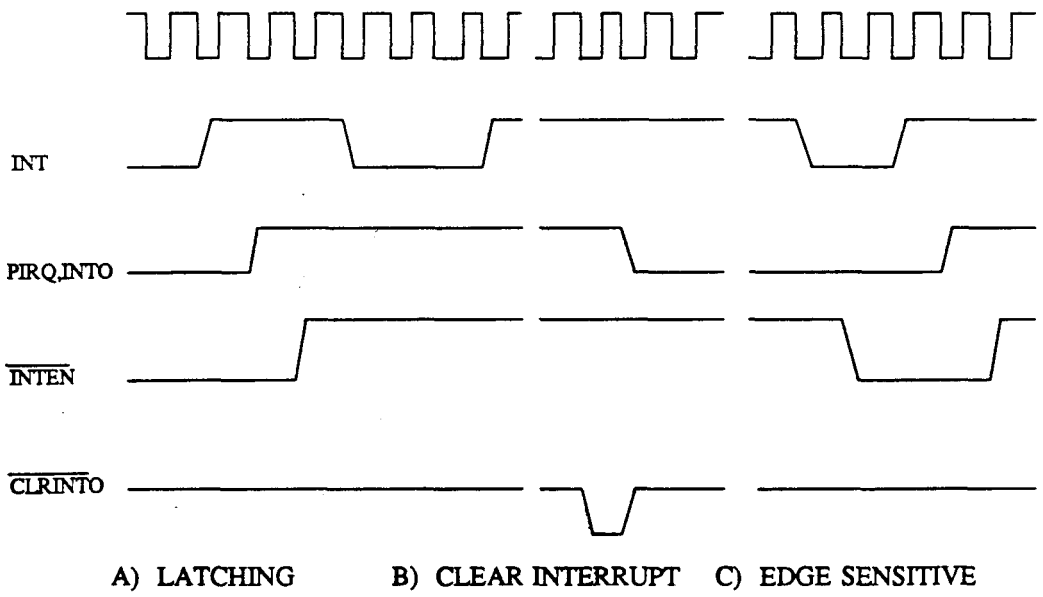


Figure 21.8 : Example interrupt cycles

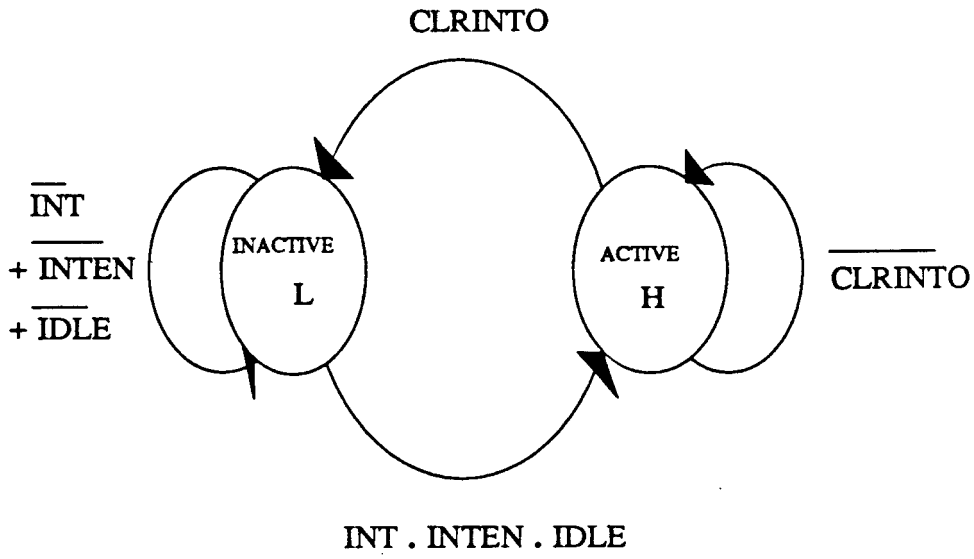


Figure 21.9: State diagram for INTO/PIRQ*

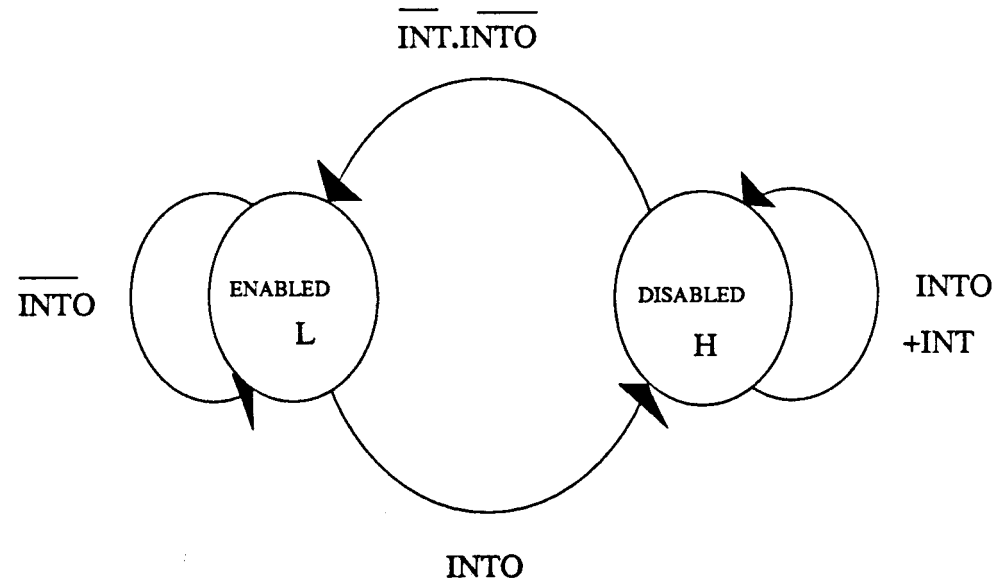


Figure 21.10: State diagram for INTEN*

Links The PCB should be viewed from the component side with the 96 way podule bus connector on the left and the rear panel on the right. When viewed like *this*, west is to *the left, east the* right, north the top and south the bottom.

LK1 and LK2 select the RAM size
If 32 kbyte devices are fitted (normally) the links should both be south. 8 kbyte devices will not normally be fitted but in this case LK1 and LK2 should be north.

LK3 to LK8 select Ethernet or Cheapernet.
For Ethernet operation the links should be west (link pin a to pin b). For Cheapernet operation the links should be east (link pin b to pin c).

LK9 is tracked south and not fitted on production units:
See data sheets for the 82502 for use.

PROM CRC calculation

The following is a code fragment in the C programming language that calculates and validates the Ethernet PROM checksum.

```
/* To calculate and check the PROM checksum */

int ROM_chk(vector)                          /* array 0..32 bytes    */
u_char vector[32];
{  register int i,j;
  register unsigned chk = -1;                /* Set the CRC register */
                                             /* to FFFFFFFF          */
  register unsigned byte;                    /* temp

  for (i = 0; i < 28; i++) {                 /* CRC on bytes 0..28   */
     byte = vector[i];
     for (j = 0; j < 8; j++) {
        if (((byte & 1) ^ (chk >> 31)) != 0)/* IF feedback = 1      */
           chk = (chk << 1) ^ (0x04C11DB7); /*    shift and EOR taps*
        else                                 /* ELSE
           chk = (chk << 1);                 /*    just shift        */
        byte = byte >> 1;                    /* next bit             */
     }
  }

/* chk is now the calculated CRC */

/* Now get CRC from PROM */

  byte = (vector[31] << 24) | (vector[30] << 16) | (vector[29] << 8)
         (vector[28] << 0);


/* Test to see if the same */

  if (byte != chk) return (FALSE); /* checksum error*/
  else return (TRUE);
}
```

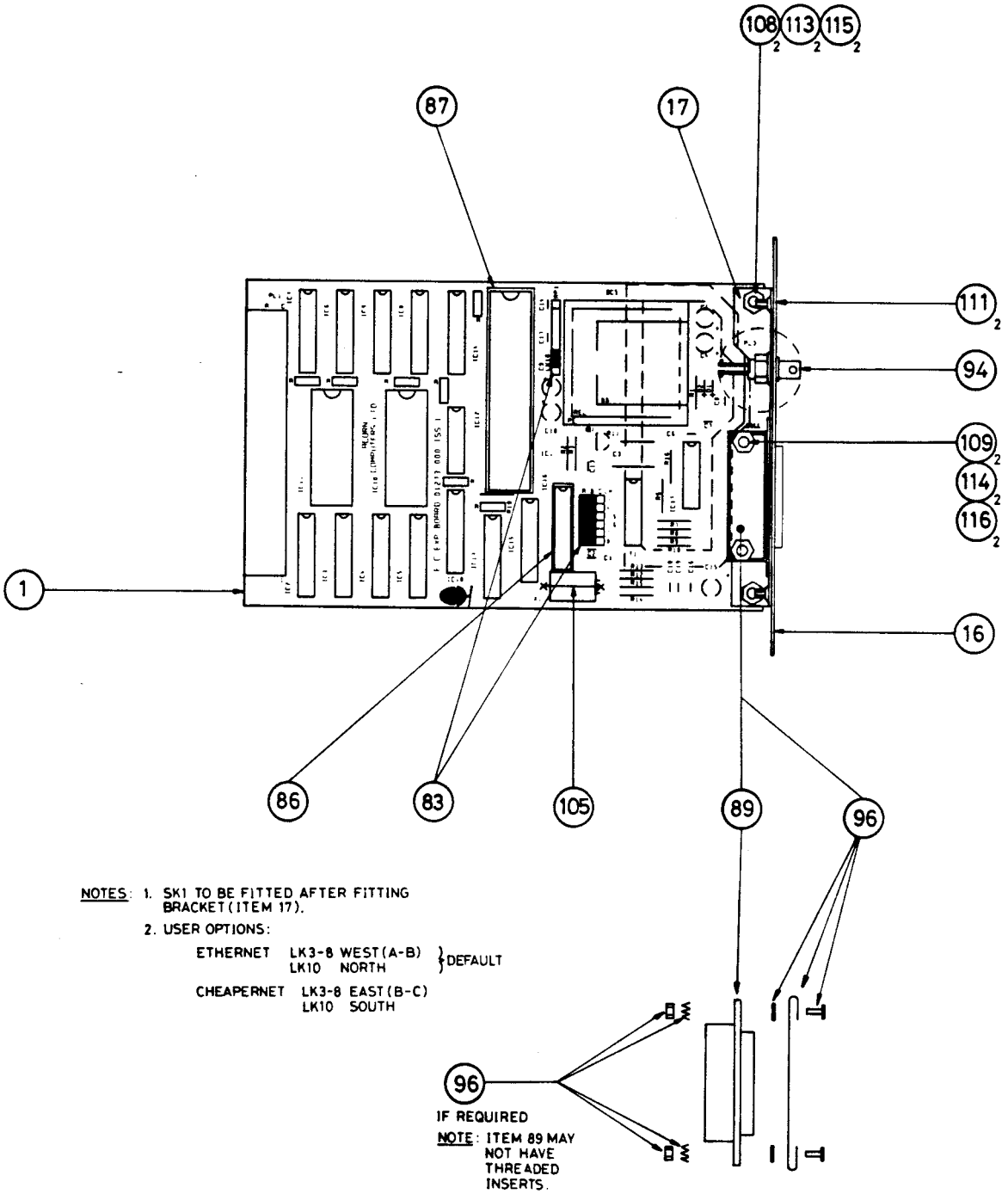
Appendix A Circuit diagrams

The Circuit diagrams in this appendix are:

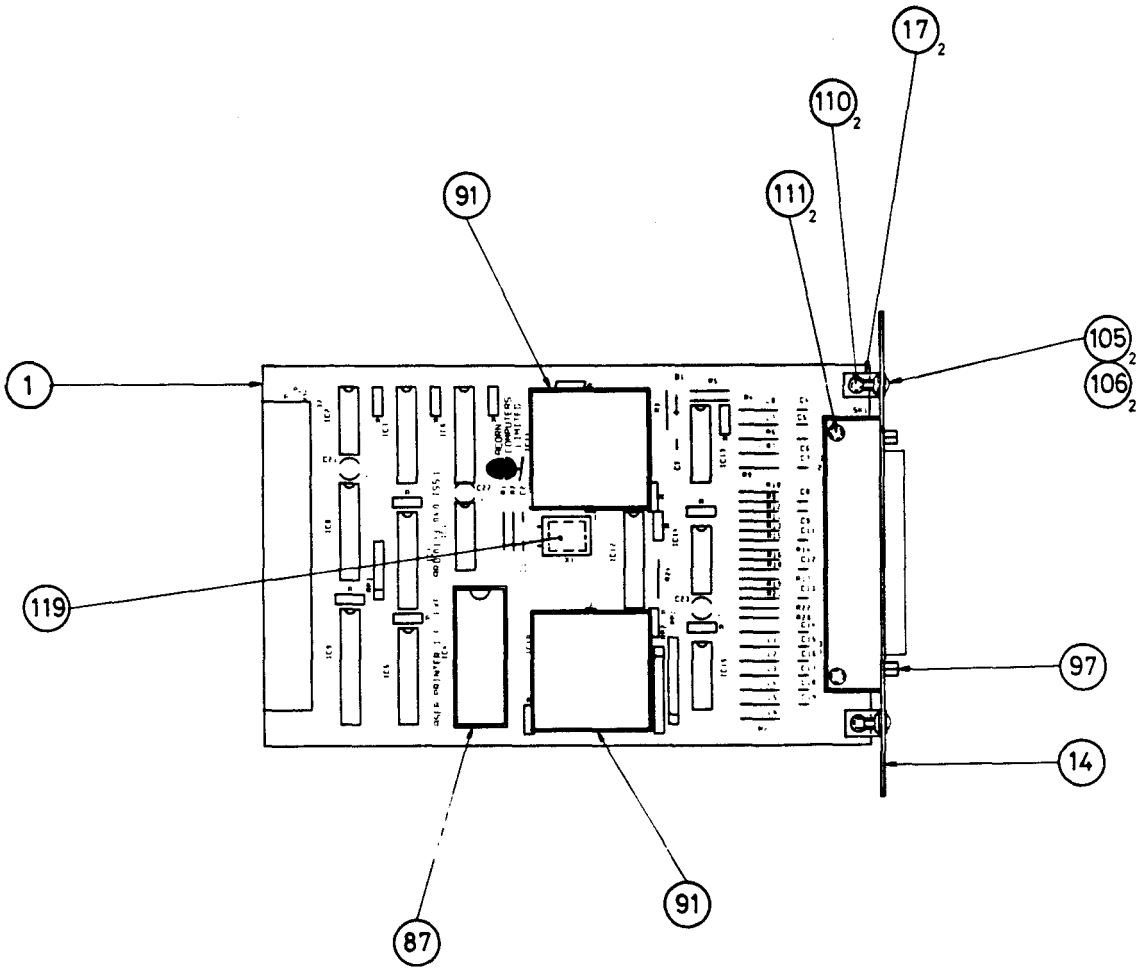
- The Main Printed Circuit Board
- The Ethernet/Cheapernet Podule
- The Laser Printer Interface Podule
- The Streamer Tape Controller Podule
- The 4 way Backplane

Appendix A : Circuit diagrams

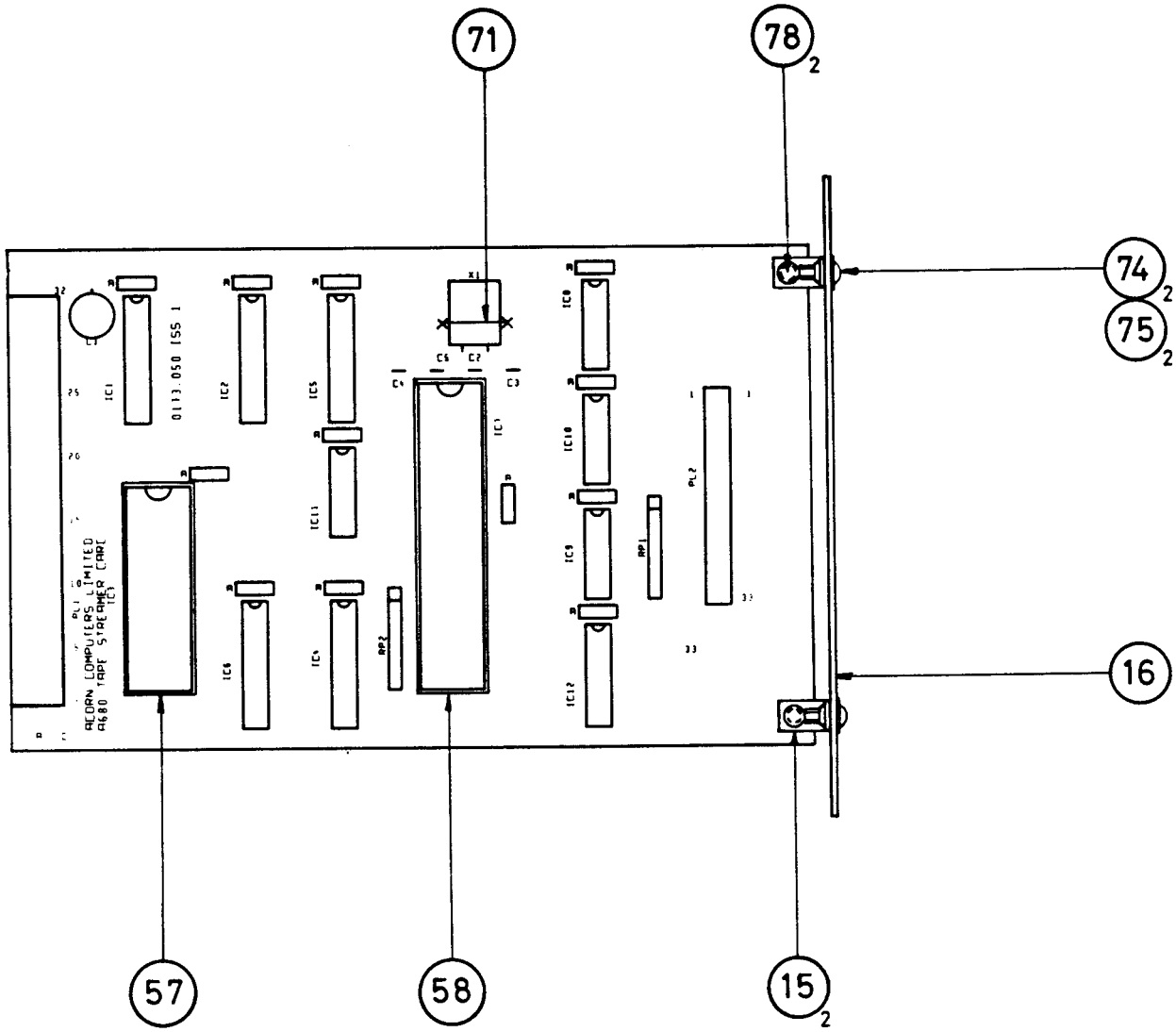
The Ethernet/Cheapernet Podule



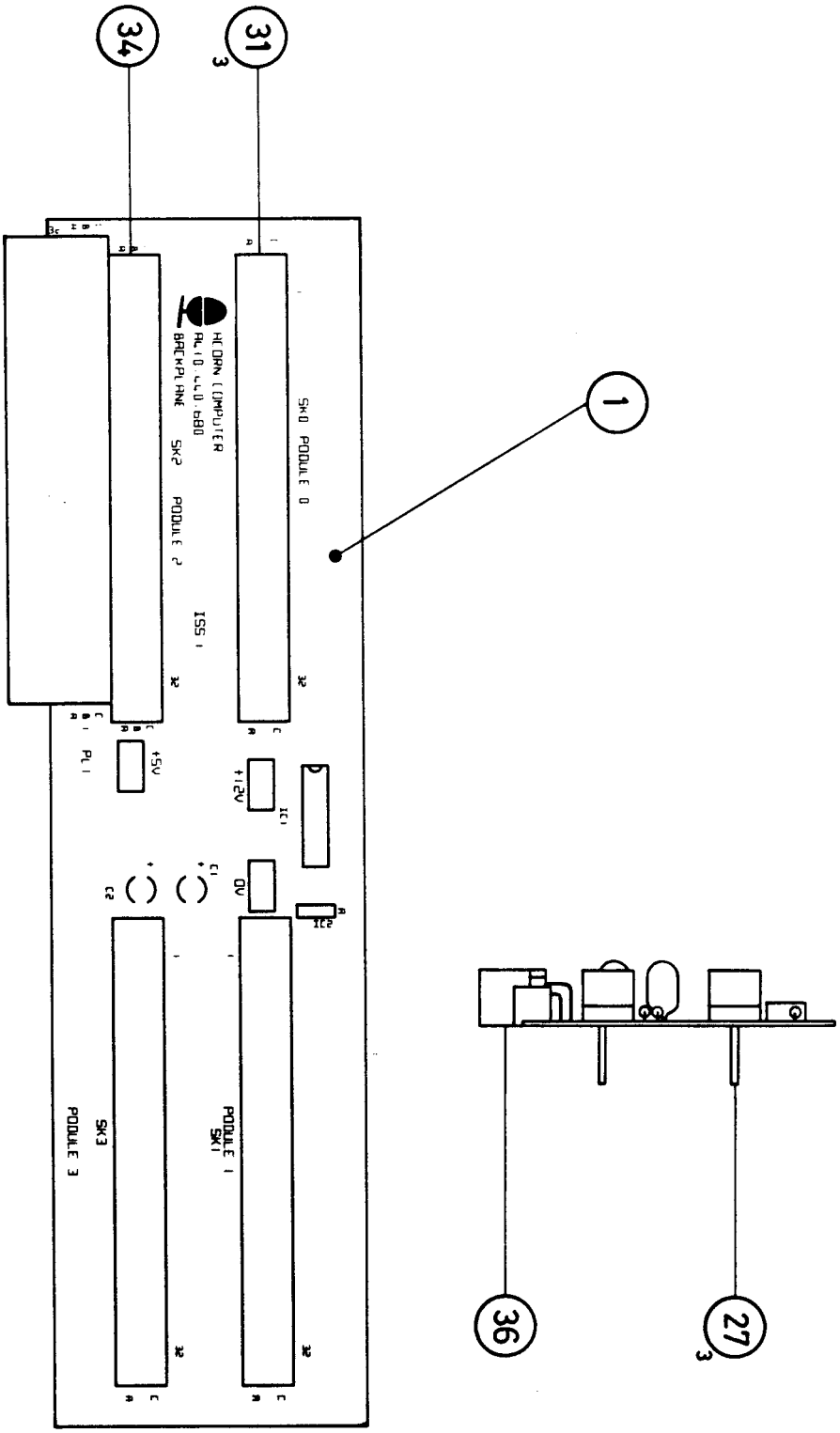
The Laser Printer Interface Podule



The Streamer Tape Controller Podule



The 4-Way Backplane



Appendix C System PCB links

These refer to the links on the system PCB. They are grouped according to the circuit diagram sheets in Appendix A.

Sheet 1	Link	Default	Function
	LK2	NF	Allows 0 V to be connected to guard.

Sheet 2	Link	Default	Function
	LK1	1-2 (tracked)	Selects video signal return to be 0 V or guard.
	LK3	2-3	Fine tunes the video shift register clock.
	LK4	1-2 (tracked)	Selects the phase relationship between the video serialiser and the system 24 MHz clock. It is normally fitted so as to link pins 2 and 3.

Sheet 3	Link	Default	Function
	LK 11	NF	Allows the real-time clock alarm function to generate an interrupt.
	LK14	NF	When installed, holds the system reset.
	LK15	1-2 (tracked)	Option not used.
	LK 16	1-2 (tracked)	Option not used.
	LK17	NF	When installed, enables the keyboard reset key.
	LK 18	1-2 (tracked)	Option not used.

Sheet 4	Link	Default	Function
	LK5	2-3	Clock selection. Selects between 16 MHz clock for SBIC and 8 MHz clock.
	LK8	NF	Factory test link.

Sheet 6

Link	Default	Function
LK10	2-3 (tracked)	Used with LK12 to select EPROM size. See the table below.
LK12	2-3 (tracked)	Used with LK10 to select EPROM size. See the table below.

Size	LK10	LK12
64K	1-2	1-2
128K	1-2	1-2
256K	1-2	2-3
512K	2-3	2-3
1024K	2-3	2-3

LK13	1-3 (tracked) 2-3 (tracked)	Selects JEDEC or ROM type EPROM (default is JEDEC)

Sheet 7

Link	Default	Function
LK6	1-2	Selects CLK24s delay. Set on test.
LK7	1-2	Selects CLK24m delay. Set on test.

The following set-up procedure should be followed to select the position of the above links:

If the system is a 4 Mbyte master only system, then IC55, IC36 and IC29 are not fitted. LK9 is made.

If the system is an 8 Mbyte dual MEMC system, IC55, IC36 and IC29 are installed. LK9 should be removed. Initially, links LK7 and LK6 should be set to link pins 1 and 2. The phase of REF8MPDm and REF8MPDs should be compared on pins 6 and 7 of J7. If they are out of phase by more than 5 ns, the phase error should be removed by adjusting links LK7 and LK6 until this is less than 5 ns. In practise it should rarely be necessary to move links LK7 and LK6 from the pin 1-2 position and this should always be tried first.

Note: The links must always be changed with the power off as the operation of IC55 is controlled by reset.

LK9	NF	Fitted if IC55 is NOT fitted. (4MByte system only)

Test points

Sheet	Test Point	Function
3	TP3	Battery voltage test point (Do NOT short to 0V)
3	TP4	Real-time clock oscillator frequency test point (Use low capacitance probe)
7	J7	System clocks (8 pins)

Appendix D Parts lists

The parts lists in this appendix are:

- The Main Printed Circuit Board
- The Ethernet/Cheapernet Podule
- The Laser Printer Interface Podule
- The Streamer Tape Controller Podule
- The 4 way Backplane

The Main Printed Circuit Board

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
1	0274,000	BARE PCB	1	
2	0174,000/A	ASSEMBLY DRAWING		1 PER BATCH
3	0174,000/C	CIRCUIT DIAGRAM		1 PER BATCH
4	0174,000/M	MODIFICATION DRAWING		1 PER BATCH
5				
6	0274,200	IC ROM 0 {0727,516 TBP}	1	IC26
7	0274,201	IC ROM 1 {0727,516 TBP}	1	IC35
8	0274,202	IC ROM 2 {0727,516 TBP}	1	IC42
9	0274,203	IC ROM 3 {0727,516 TBP}	1	IC51
10	0274,204	IC GAL 1 {0760,200 TBP}	1	IC30
11	0274,205	IC GAL 2 {0760,201 TBP}	1	IC25
12	0274,206	IC GAL 3 {0760,200 TBP}	1	IC15
13	0274,207	IC GAL 4 {0760,200 TBP}	1	IC9
14	0274,208	IC GAL 5 {0760,200 TBP}	1	IC27
15	0274,209	IC GAL 6 {0760,200 TBP}	1	IC31
16	0274,210	IC GAL 7 {0760,200 TBP}	1	IC23
17	0274,211	IC GAL 8 {0760,201 TBP}	1	IC40
18	0274,212	IC GAL 9 {0760,200 TBP}	1	IC55
19	0274,213	IC GAL 10 {0760,201 TBP}	2	IC58,66
20	0274,214	IC GAL 11 {0760,201 TBP}	1	IC20
21	0274,215	IC GAL 12 {0760,202 TBP}	2	IC52,62
22	0274,216	IC GAL 13 {0760,201 TBP}	1	IC17
23	0274,217	IC GAL 14 {0760,200 TBP}	1	IC22
24	0274,218	IC GAL 15 {0760,200 TBP}	1	IC19
25	0274,219	IC GAL 16 {0760,200 TBP}	1	IC72
26				
27				
28				
29	0274,700	MAIN PCB BACK PANEL	1	
30				
31	0174,731	BNC CABLE ASSEMBLY	2	
32				
33	2201,375	IC MEMC 1A (PLSTC)	2	IC69,70
34				
35	2201,365	IC ARM (2um PLSTC)	1	IC68
36				
37	2201,367	IC VIDC 1A (PLSTC)	1	IC28
38	2201,368	IC IOC (PLSTC)	1	IC100
39				
40				
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
41				
42				
43				
44				
45	0502,100	RES 10R C/MF 5% 0W25	3	R11,62,127
46	0502,101	RES 100R C/MF 5% 0W25	4	R156,157,164,172
47	0502,102	RES 1K C/MF 5% 0W25	1	R107
48	0502,103	RES 10K C/MF 5% 0W25	36	R12,17,37,39,41,43,55,56 R59,70-73,77,81,83,84,86 R88,94,100,104,105,112 R113,115-118,141,152,160 R161,170,171,176
49				
50				
51	0502,104	RES 100K C/MF 5% 0W25	3	R66,102,179
52	0502,121	RES 120R C/MF 5% 0W25	1	R2
53	0502,122	RES 1K2 C/MF 5% 0W25	11	R18,19,38,45,57,126,139 R150,167,168,175
54				
55				
56				
57				
58	0502,220	RES 22R C/MF 5% 0W25	6	R4-9
59	0502,221	RES 220R C/MF 5% 0W25	1	R1
60	0502,222	RES 2K2 C/MF 5% 0W25	3	R95,151,182
61	0502,271	RES 270R C/MF 5% 0W25	12	R15,42,58,61,69,82,90-93 R103,166
62				
63				
64	0502,330	RES 33R C/MF 5% 0W25	16	R44,74-76,78-80,87,89 R96-98,101,114,121,153
65				
66	0502,331	RES 330R C/MF 5% 0W25	1	R60
67				
68				
69	0502,470	RES 47R C/MF 5% 0W25	3	R63-65
70	0502,471	RES 470R C/MF 5% 0W25	2	R13,85
71	0502,472	RES 4K7 C/MF 5% 0W25	11	R46-54,109,119
72	0502,473	RES 47K C/MF 5% 0W25	2	R146,148
73	0502,562	RES 5K6 C/MF 5% 0W25	1	R16

| ITEM | PART NO | DESCRIPTION | QTY | REMARKS |

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
74				
75	0502,680	RES 68R C/MF 5% 0W25	42	R3,14,67,68,99,106,110 R111,120,122-125,130,133 R136-138,140,142-145,147 R149,154,155,158,159,162 R163,165,169,173,174,177 R178,180,181,183 R184 (MOD DRG).
76				
77	0502,681	RES 680R C/MF 5% 0W25	1	R10
78				
79				
80				
81				
82				
83	0507,279	RES 2R7 MF 1% 0W25	17	R20-36
84				
85	0507,393	RES 39K MF 1% 0W25 E24	2	R128,131
86				
87	0507,472	RES 4K7 MF 2% 0W25 E24	2	R129,132
88				
89	0507,561	RES 560R MF 1% 0W25 E24	2	R134,135
90				
91				
92				
93				
94				
95				
96				
97	0571,220	RES 22R NET DIL 2% 16P	1	RN1
98				
99	0571,330	RES 33R NET DIL 2% 16P	4	RN3-6
100				
101	0571,680	RES 68R NET DIL 2% 16P	2	RN7,8
102				
103				
104				
105				
106	0573,472	RES 4K7 NET DIL 5% 16P	1	RN9
107				
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
108				
109				
110				
111				
112	0590,019	RES 1K0x7 NET SIL 8P 2%	1	RN10
113	0590,103	RES 10Kx8 NET SIL 10% 9P	1	RN2
114				
115				
116				
117				
118				
119				
120				
121				
122	0629,010	CPCTR CPLT 10n 30V 80%	1	C83
123				
124				
125				
126	0630,100	CPCTR CPLT 1n 30V 10%	4	C45,52-54
127	0630,220	CPCTR CPLT 2n2 30V 10%	8	C4-11
128				
129				
130				
131				
132				
133				
134	0631,022	CPCTR CPLT 22p 30V 2%	17	C19-27,30-37
135				
136	0631,033	CPCTR CPLT 33p 30V 2%	1	C13
137	0631,056	CPCTR CPLT 56p 30V 2%	2	C1,86
138	0631,068	CPCTR CPLT 68p 30V 2%	1	C87
139	0631,100	CPCTR CPLT 100p 30V 2%	6	C2,3,12,14-16
140				
141	0631,270	CPCTR CPLT 270p 30V 2%	1	C18
142	0631,330	CPCTR CPLT 330p 30V 2%	1	C157 (MOD DRG)
143	0635,100	CPCTR ALEC 10u 16V RAD	24	C38,40,42-44,46-48,57,69 C74,79,80-82,"B" (x8)
144				
145				
146				

ITEM	PART NO	DESCRIPTION	QTY	REMARKS

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
147	0635,227	CPCTR ALEC 220u 16V 20%	4	C62,66,67,72
148				
149				
150				
151	0650,104	CPCTR MPSTR 100n 50V 10%	2	C75,77
152	0650,223	CPCTR MPSTR 22n 50V 10%	2	C70,78
153				
154				
155				
156	0680,006	CPCTR DCPLR 33/47n 0.2"	173	C17,28,29,39,41,49,50 C56,60,61,63-65,68 C71,73,76,85,"A" (x156)
157				
158				
159				
160	0699,001	CPCTR TRMR 2/22p 250V	1	C58
161				
162	(0701,394)	IC 33C93A SCSI 40/0.6"	1	IC10
163				
164				
165	0704,105	IC 4464 DRAM 120nS 64Kx4	8	IC34,39,44,48,53,59,63,67
166	0704,115	IC 1M X 1 DRAM 100nS ZIP	64	IC75,76,79-82,84-91,93-96 IC98,99,101,102,104-109 IC111-118,120-129,133-138 IC141,142,144-147,149-154
167				
168				
169	0708,530	IC 8530APC SCC 40/0.6"	1	IC18
170				
171	0708,583	IC 8583 RTC RAM 8/0.3"	1	IC54
172				
173				
174	0709,232	IC 92C32 FDDS 8/0.3"	1	IC148
175				
176	0709,793	IC 9793 FDC 5V 40/0.6"	1	IC119
177				
178				
179				
180				
181	0721,001	IC DLY 50nS 5T 8/0.3"	1	IC21

| ITEM | PART NO | DESCRIPTION | QTY | REMARKS |

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
182	0721,002	IC DLY 20nS 10T 14/0.3"	2	IC29,36
183				
184				
185	0735,239	IC MAX 239 RS232 24/0.3"	1	IC1
186				
187				
188	0740,006	IC 7406 TTL 14/0.3"	2	IC4,131
189				
190				
191				
192				
193				
194				
195	0742,014	IC 74LS14 TTL 14/0.3"	1	IC16
196	0742,646	IC 74LS646 TTL 24/0.3"	1	IC5
197				
198				
199				
200				
201				
202				
203	0747,004	IC 74HC04 CMOS 14/0.3"	1	IC139
204	0747,014	IC 74HC14 CMOS 14/0.3"	1	IC110
205				
206	0747,139	IC 74HC139 CMOS 16/0.3"	1	IC83
207	0747,174	IC 74HC174 CMOS 16/0.3"	1	IC8
208				
209	0747,573	IC 74HC573 CMOS 20/0.3"	2	IC77,78
210	0747,574	IC 74HC574 CMOS 20/0.3"	3	IC46,50,130
211				
212	0748,000	IC 74F00 TTL 14/0.3"	1	IC6
213	0748,004	IC 74F04 TTL 14/0.3"	1	IC13
214	0748,074	IC 74F74 TTL 14/0.3"	3	IC11,14,49
215	0748,112	IC 74F112 TTL 16/0.3"	1	IC140
216	0748,166	IC 74F166 TTL 16/0.3"	1	IC2
217	0748,174	IC 74F174 TTL 16/0.3"	1	IC71
218	0748,175	IC 74F175 TTL 16/0.3"	1	IC41
219				
220				
221	0749,003	IC 74HCT03 CMOS 14/0.3"	1	IC97
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
222	0749,008	IC 74HCT08 CMOS 14/0.3"	1	IC3
223				
224	0749,125	IC 74HCT125 CMOS 14/0.3"	1	IC143
225				
226	0749,245	IC 74HCT245 CMOS 20/0.3"	1	IC103
227				
228	0749,573	IC 74HCT573 CMOS 20/0.3"	3	IC12,73,74
229				
230				
231				
232	0750,004	IC 74AC04 CMOS 14/0.3"	1	IC60
233	0750,008	IC 74AC08 CMOS 14/0.3"	1	IC64
234	0750,011	IC 74AC11 CMOS 14/0.3"	2	IC24,132
235	0750,574	IC 74AC574 CMOS 20/0.3"	1	IC57
236				
237				
238	0751,000	IC 74ACT00 CMOS 14/0.3"	1	IC7
239	0751,008	IC 74ACT08 CMOS 14/0.3"	1	IC61
240				
241	0751,245	IC 74ACT245 CMOS 20/0.3"	4	IC33,38,43,47
242				
243	0751,646	IC 74ACT646 CMOS 24/0.3"	4	IC37,45,56,65
244				
245				
246				
247				
248	0770,386	IC LM386 AUDIO AMP	1	IC92
249				
250	0778,007	VOLT REG 78L05A +5V/0.1A	1	Q3
251				
252				
253	0780,239	TRANS BC239 NPN	1	Q2
254				
255				
256				
257				
258				
259				
260				
261				
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
262	0783,904	TR. 2N3904 NPN TO92 CBE	1	Q1
263	0790,048	DIODE BAT85 SBL	1	D3
264				
265				
266				
267	0794,001	DIODE 1N4001 SI 50V 1A	6	D5-8,11,12
268				
269	0794,148	DIODE 1N4148 SI	5	D1,2,4,9,10
270				
271				
272				
273				
274				
275	0799,101	IC TIL311 DISPLAY	1	IC32
276				
277				
278				
279				
280				
281	0800,030	CONR 50W HDR IDC ST 4WALL	1	J9
282				
283	0800,050	CONR 2W WAFR 0.1" ST PCB	1	LK17
284	0800,051	CONR 3W WAFR 0.1" ST PCB	2	LK3,5
285				
286	0800,070	CONR 2W SHUNT 0.1"	5	LK3,5-8
287				
288				
289				
290				
291				
292				
293				
294	0800,132	SKT IC 32/0.6" SUPA	4	IC26,35,42,51
295				
296	0800,169	SKT IC 68P PLCC	4	IC28,69,70,100
297	0800,185	SKT IC 84P PLCC	1	IC68
298				
299				
300				
301	0800,203	FSTN TAB 6,3x0,8 ST PCB	4	FT3-6
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
302	0800,291	CONRD 9W PLG RAPCB+RFI+L	1	J1
303	0800,293	CONRD 25W SKT RAPCB+RFI+L	1	J2
304				
305				
306	0800,371	CONR 50W SKT DELTA RA PCB	1	J3
307				
308				
309	0800,408	CONR 96W SKT ST ABC PCB	1	PL1
310	0800,457	CONR 10W WAFR 0.1" ST PCB	1	J7
311	0800,458	CONR 2W WAFR 0.1" ST LK	5	J4(x2),6,10/11
312				
313				
314				
315				
316				
317				
318				
319	0800,471	CONR 5W WAFR 0.1" ST LK	1	J12
320	0800,880	CONR 6W WAFR 2ROW 0.1"P	1	LK8
321	0800,884	CONR 22W WAFR 0.1" 2ROW	2	LK6,7
322				
323				
324				
325				
326				
327				
328	0803,102	CONR 34W BOX IDC LP ST	1	J8
329				
330				
331				
332	0815,210	FUSE 500mA F 20x5mmD LBC	1	F1
333	0815,305	FUSE 2A LBC AX	1	F2
334	0815,910	FUSE CLIP 5mmD SE PCB	2	FOR FUSE (F1)
335				
336				
337				
338	0820,036	XTAL 3.6864 MHz HC18	1	X3
339				
340				
341				
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
342	0820,960	XTAL OSC 96MHZ ECL 14/.3"	1	X1
343				
344				
345				
346	0821,327	XTAL 32.768KHz CC 0.05"P	1	X2
347				
348				
349				
350	0860,005	CHOKE RF 33uH AX Q=45	2	L2,3
351				
352	0860,016	CHOKE RFI FERRITE AX	1	L1
353				
354				
355	0870,164	WIRE 1/0.6mm PVC GRN	400mm	MOD DRG
356	0870,422	WIRE 25SWG CPR TIN	A/R	USE ON X2,3
357				
358	0882,128	SCW M3x8 PAN HD POSI Z&P	2	USE WITH J3
359	0882,902	NUT M3 STL FULL Z/PAS	2	USE WITH J3
360	0882,962	WSHR M3 PLN STL Z/PAS	2	USE WITH J3
361				
362				
363				
364				
365				
366				
367				
368				
369				
370				
371				
372				
373				
374				
375				
376				
377				
378				
379				
380				
381				

| ITEM | PART NO | DESCRIPTION | QTY | REMARKS |

The Ethernet/Cheapernet Podule

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
1	0273,000/D	BARE PCB	1	PCB ASSY
2	0173,000/A	ASSEMBLY DRAWING		1 PER BATCH
3	0173,000/C	CIRCUIT DIAGRAM		1 PER BATCH
4				
5				
6				
7				
8	0273,200	IC GAL 1 {0760,200 TBP}	1	IC13
9	0273,201	IC GAL 2 {0760,200 TBP}	1	IC14
10	0273,202	IC GAL 3 {0760,200 TBP}	1	IC15
11	0273,203	IC PROM {0702,719 TBP}	1	IC12
12				
13				
14				
15				
16	0273,700	ETHER/CHEAPERNET REAR PNL	1	
17	0273,701	PCB SUPPORT MOUNTING BRKT	1	
18				
19				
20				
21				
22				
23				
24				
25				
26				
27				
28	0502,472	RES 4K7 C/MF 5% 0W25	1	R18
29				
30	0506,157	RES 39R2 MF 1% 0W25 E96	4	R12-15
31	0506,161	RES 43R2 MF 1% 0W25 E96	4	R7-10
32	0506,186	RES 78R7 MF 1% 0W25 E96	1	R6
33				
34	0509,000	RES 243R MF 0%5 0W25	3	R2,3,16
35				
36	0511,105	RES 1M0 HIVOLT 5% 0W25	1	R11
37				
38	0590,070	RES 10Kx5 NET SIL 6P 5%	1	RP1
39				
40				
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
41				
42				
43	0631,033	CPCTR CPLT 33p 30V 2%	2	C1,2
44				
45	0635,470	CPCTR ALEC 47uF 16V RAD	5	C4,5,9,10,15
46				
47	0637,224	CPCTR CML 220n 25V 80%	1	C8
48				
49	0643,103	CPCTR CER 10n 100V 20%	2	C18,19
50				
51	0650,223	CPCTR MPSTR 22n 50V 10%	1	C13
52				
53	0670,103	CPCTR CLASY 10n 250V 20%	1	C3
54				
55	0680,002	CPCTR DCPLR 33/47n 0.2"	12	"A",C6,7,14,16,17
56				
57				
58				
59				
60				
61	0702,118	IC 62256 SRAM 100nS 32Kx8	2	IC10,11
62				
63	0706,856	IC 82501 SIA NMOS 20/0/3"	1	IC16
64	0706,857	IC 82502 TRAN MOS 16/0.3"	1	IC17
65	0706,858	IC 82586 LAN NMOS 48/0.6"	1	IC1
66				
67	0749,244	IC 74HCT244 CMOS 20/0.3"	2	IC2,3
68	0749,245	IC 74HCT245 CMOS 20/0.3"	4	IC6,7,8,9
69	0749,573	IC 74HCT573 CMOS 20/0.3"	2	IC4,5
70				
71	0751,240	IC 74ACT240 CMOS 20/0.3"	1	IC18
72				
73	0778,002	DC/DC CONV 12V TO 5V,10V	1	DC1 (was DC)
74				
75	0780,239	TRANS BC239 NPN TO92 EBC	1	Q1 (was TR1)
76				
77	0794,022	DIODE IN4150 SI 50V DO35	2	D1,2
78				
79				
80				
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
81				
82	0800,051	CONR WAFR 3W 0.1" ST PCB	1	LK10
83	0800,070	CONR 2W SHUNT 0.1"	7	LK3-8,10
84				
85				
86	0800,121	SKT IC 20/0.3" SUPA	1	USE ON IC16
87	0800,149	SKT IC 48/0.6" SUPA	1	USE ON IC1
88				
89	0800,270	CONR 15W SKT RA PCB+RFI	1	SK1 (was PL2)
90				
91	0800,404	CONR 64W PLG RA AC	1	PL1
92	0800,450	CONR WAFR 6W 0.1" ST PCB	3	LK3-8
93				
94	0800,601	CONR BNC SKT PNL 50R INSU	1	PL3
95				
96	0800,986	15W D SLIDE LOCK ASSY	1	USE ON SK1
97	0815,306	FUSE 50/63mA LBC AX 9x3,2	1	R1
98				
99	0820,201	XTAL 20MHZ HC18 20PF P/L	1	X1
100				
101				
102	0865,601	ISO TRANS 16PIN DIL 0.3"	1	T1
103				
104				
105	0870,420	WIRE 22SWG CPR TIN	A/R	USE ON X1,PL3
106				
107				
108	0882,111	SCW M2.5x6 PAN HD POSI	2	USE ON 1,17
109	0882,123	SCW M3x10 PAN HD POSI	2	USE ON 1,17,89
110				
111	0882,211	SCW M2.5x6 CSK HD POSI	2	USE ON 16,17
112				
113	0882,901	NUT M2.5 STL FULL Z/PAS	2	USE ON 108
114	0882,902	NUT M3 STL FULL Z/PAS	2	USE ON 96,109
115	0882,971	WSHR M2.5 SPRF IT STL	2	USE ON 108
116	0882,972	WSHR M3 SPRF IT STL	2	USE ON 96,109
117				
118				
119				
120				

| ITEM | PART NO | DESCRIPTION | QTY | REMARKS |

The Laser Printer Interlace Podule

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
1	0273,040	BARE PCB	1	
2	0173,040/A	ASSEMBLY DRAWING		1 PER BATCH
3	0173,040/C	CIRCUIT DIAGRAM		1 PER BATCH
4				
5				
6				
7	0273,240	IC ROM {0727,128 TBP}	1	IC4
8	0273,241	IC GAL 1 {0760,200 TBP}	1	IC8
9	0273,242	IC GAL 2 {0760,201 TBP}	1	IC9
10	0273,243	IC GAL 3 {0760,200 TBP}	1	IC12
11				
12				
13				
14	0273,740	LASER PCB BACKPANEL	1	
15				
16				
17	0276,204	PODULE PCB BRACKET (STD)	2	
18				
19				
20	2201,367	IC VIDC 1A JED B	1	IC11
21	2201,368	IC IOC JED B	1	IC10
22				
23				
24				
25	0502,101	RES 100R C/MF 5% 0W25	4	R9,12,15,18
26	0502,103	RES 10K C/MF 5% 0W25	2	R4,5
27	0502,104	RES 100K C/MF 5% 0W25	1	R1
28				
29	0502,151	RES 150R C/MF 5% 0W25	1	R7
30				
31	0502,221	RES 220R C/MF 5% 0W25	3	R2,23,24
32	0502,270	RES 27R C/MF 5% 0W25	1	R21
33				
34	0502,331	RES 330R C/MF 5% 0W25	6	R6,8,11,14,17,20
35				
36	0502,471	RES 470R C/MF 5% 0W25	6	R3,10,13,16,19,22
37				
38	0590,052	RES 220Rx5 NET SIL 6P 5%	1	RP3
39	0590,222	RES 2K2 NET SIL 10% 9P	2	RP1,2
40				
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
41				
42	0610,010	CPCTR TANT 10u 10V 20%	2	C22,23
43	0611,470	CPCTR TANT 47u 16v 20%	1	C21
44				
45	0629,010	CPCTR CPLT 10n 30V 80%	4	C8,9,11,12
46				
47				
48	0630,100	CPCTR CPLT 1n0 30V 10%	2	C6,7
49	0630,220	CPCTR CPLT 2n2 30V 10%	1	C13
50				
51				
52	0631,010	CPCTR CPLT 10p 30V 2%	1	C1
53	0631,033	CPCTR CPLT 33p 30V 2%	1	C2
54	0631,068	CPCTR CPLT 68p 30V 2%	8	C4,5,14,15,16,17,18,19
55	0631,100	CPCTR CPLT 100p 30V 2%	1	C3
56				
57				
58				
59				
60				
61	0680,002	CPCTR DCPLR 33/47n 0.2"	14	A
62				
63				
64				
65				
66				
67	0735,116	IC 75116 LINE TRANSCEIVER	1	IC13
68				
69	0740,016	IC 7416 TTL 14/0.3"	1	IC15
70				
71	0742,014	IC 74LS14 TTL 14/0.3"	1	IC14
72				
73	0747,004	IC 74HC04 CMOS 14/0.3"	1	IC1
74				
75	0749,245	IC 74HCT245 CMOS 20/0.3"	1	IC3
76	0749,573	IC 74HCT573 CMOS 20/0.3"	3	IC5,6,7
77				
78	0750,008	IC 74AC08 CMOS 14/0.3"	1	IC2
79				
80	0794,148	DIODE SI 1N4148	1	D1
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
81				
82				
83				
84				
85				
86				
87	0800,129	SKT IC 28/0.6" SUPA	1	USE ON IC4
88				
89				
90				
91	0800,169	SKT IC 68P PLCC	2	USE ON IC10,11
92				
93	0800,296	CONRD 37W RA PCB RFI	1	SK1
94				
95	0800,409	CONR 64W PLG RA AC PCB	1	PL1
96				
97	0800,983	CONRD 4-40UNC JKSKTKIT	1	USE ON SK1
98				
99				
100				
101	0820,220	XTAL 22.365760 MHz HC18/U	1	X1
102				
103				
104				
105	0882,111	SCW M2,5x6 PAN HD POSI	2	USE ON ITEM 14,17
106	0882,967	WSHR M2,5 PLN STL Z/PASS	2	USE ON ITEM 105
107				
108				
109				
110	0884,042	RIVET POP DOME 3,2D & THK	2	USE ON ITEM 17
111	0884,044	RIVET POP 3,2D FOR 'D'	2	USE ON SK1
112				
113				
114				
115	0860,011	CHOKE RF u33H AX Q=30	8	L1-8
116				
117				
118				
119	0895,081	FOAM PAD SF-ADH DBL SIDED	1	USE ON X1
120				
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

The Streamer Tape Controller Podule

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
1	0273,050/D	BARE PCB	1	PCB ASSY
2	0173,050/A	ASSEMBLY DRAWING		1 PER BATCH
3	0173,050/C	CIRCUIT DIAGRAM		1 PER BATCH
4				
5				
6				
7	0273,250	IC ROM {0727,128 TBP}	1	IC3
8	0273,251	IC GAL 1 {0760,200 TBP}	1	IC2
9	0273,252	IC GAL 2 {0760,200 TBP}	1	IC5
10				
11				
12				
13				
14				
15	0276,204	PODULE PCB BRACKET (STD)	2	
16	0276,228	PODULE (PLAIN) REARPANEL	1	
17				
18				
19				
20	0590,009	RES 150Rx7 NET SIL 8P 2%	1	RP1
21	0590,028	RES 4K7x7 NET SIL 8P 2%	1	RP2
22				
23				
24				
25	0631,027	CPCTR 27p CPLT 30V 2%	4	C2,3,4,5
26				
27	0642,101	CPCTR 100u ALEC 25V RAD	1	C1
28				
29	0680,002	CPCTR 33/47n DCPLR 0.2"	12	"A"
30				
31				
32				
33				
34				
35	xxxx,xxx	IC 72067 FDC	1	IC7
36				
37				
38	0740,006	IC 7406 TTL 14/0.3"	1	IC10
39	0740,038	IC 7438 TTL 14/0.3"	1	IC8
40				
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
41				
42	0749,008	IC 74HCT08 CMOS 14/0.3"	1	IC11
43	0749,014	IC 74HCT14 CMOS 14/0.3"	1	IC9
44	0749,157	IC 74HCT157 CMOS 16/0.3"	1	IC12
45	0749,245	IC 74HCT245 CMOS 20/0.3"	1	IC1
46	0749,273	IC 74HCT273 CMOS 20/0.3"	2	IC4,6
47				
48				
49				
50				
51				
52				
53				
54				
55				
56				
57	0800,131	SKT IC 32/0.6" NORM	1	USE WITH IC3
58	0800,148	SKT IC 48/0.6" NORM	1	USE WITH IC7
59				
60				
61	0800,409	CONR 64W PLG RA AC PCB	1	PL1
62				
63				
64	0803,102	CONR 34W BOX IDC LP ST	1	PL2
65				
66				
67				
68	0820,xxx	XTAL 32 MHz HC18/U	1	X1
69				
70				
71	0870,420	WIRE 22SWG CPR TIN	A/R	USE WITH X1
72				
73				
74	0882,111	SCW M2,5x6 PAN HD POSI	2	USE WITH ITEM 12,15
75	0882,967	WSHR M2,5 PLN STL Z/PASS	2	USE WITH ITEM 12,15
76				
77				
78	0884,042	RIVET POP DOME 3,2D & THK	2	USE WITH ITEM 1,15
79				
80				

| ITEM | PART NO | DESCRIPTION | QTY | REMARKS |

The 4-Way Backplane

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
1	0283,040	BARE PCB	1	
2	0174,040/A	ASSEMBLY DRAWING		1 PER BATCH
3	0183,040/C	CIRCUIT DIAGRAM		1 PER BATCH
4				
5				
6				
7				
8	0274,240	IC GAL {0760,200 TBP}	2	IC2,3
9				
10				
11				
12				
13				
14				
15	0635,228	CPCTR ALEC 220u 16V 20%	2	C1,2
16				
17	0680,002	CPCTR DCPLR 33/47n 0.2"	2	"A"
18				
19				
20				
21				
22	0747,139	IC 74HC139 CMOS 16/0.3"	1	IC1
23				
24				
25				
26				
27	0800,203	FSTN TAB 6,3x0,8 ST PCB	3	0V,+5V,+12V
28				
29				
30				
31	0800,400	CONR 64W SKT ST AC PCB SH	3	SK0,1,3
32				
33				
34	0800,408	CONR 96W SKT ST ABC PCB	1	SK2
35				
36	0800,410	CONR 96W PLG RA ABC PCB	1	PL1
37				
38	0502,103	RES 10K C/MF 5% 0W25	5	R1,2,3,4,5
39				
40				
ITEM	PART NO	DESCRIPTION	QTY	REMARKS

Appendix E Device data sheets

INTEL 82586 LAN Coprocessor
INTEL 82501 Ethernet Serial Interface
INTEL 82502 Ethernet Transceiver Chip

FD1793-02 / Western Digital Floppy Disc Controller
Z8530 SCC / Zilog
PCF 8583 256 x 8 bit Static RAM / Mullard

Western Digital WD33C93 SBIC Data Sheet
Western Digital WD33C93 A Data Sheet
Western Digital SBIC Applications Notes
NEC µPD 72067 Floppy Disc Controller

Appendix F Connectors

I/O connectors

The following are positioned on the system board back panel:

- serial interface - RS232 (9 way D-type (male))
- printer port - 25 way D-type (female)
- SCSI interface - single ended (50 way Type 57 Delta or IDC)
- video sync - BNC
- video signal - BNC
- laser printer interface - Canon video interface (37-way D-type).

The following are incorporated into the PSU back panel:

- mains inlet - IEC 320/CEE22
- mains outlet - IEC 320/CEE22
- on/off switch.

The following are positioned at the front:

- keyboard - 6 way miniature DIN socket.

Printer connector

Pin	Name	Pin	Name
1	STROBE*	14	AUTOLF*
2	PD0	15	ERROR*
3	PD1	16	PRST*
4	PD2	17	SELECTIN*
5	PD3	18	0V
6	PD4	19	0V
7	PD5	20	0V
8	PD6	21	0V
9	PD7	22	0V
10	ACK*	23	0V
11	BUSY	24	0V
12	PE	25	0V
13	SELECT		

Floppy disc drive connector

Pin	Name	Option(S)	Pin	Name	Option(s)
1	DCRST*	0V	18	DM IN*	
2	DCIRQ*	SIZE	19	0V	
3	0V	20		STEP*	
4	IN USE*		21	0V	
5	5V 0V	22		WRITE DATA*	
6	5V	23		0V	
7	5V 0V	24		WRITE GATE	
8	INDEX*		25	0V	
9	5V 0V	26		TRACK00	
10	SEL0*		27	0V	
11	0V		28	WRITE PROT	
12	SEL1*		29	0V	
13	0V		30	READ DATA	
14	5V		31	0V	
15	0V		32	SIDE	
16	MOTOR ON*		33	0V	
17	0V		34	READY	DCIRQ*, 0V

Serial port connector

Pin	Name
1	DCD
2	RxD
3	TxD
4	DTR
5	0V
6	DSR
7	RTS
8	CTS
9	RI

Keyboard connector

Pin	Name
1	Reset
2	N.C.
3	0V
4	5V
5	Serial data from keyboard
6	Serial data to keyboard

Video and sync connectors

Video		Sync	
Center	Video	Center	Sync
Outer		0V Outer	0V

Cartridge tape connector

Pin	Function	
2	Pulled to +5 V via 150 Ohm	I/P
4	No connection	
6	Drive select 4	I/P
8	Index	0/P
10	Drive select 1	I/P
12	Drive select 2	I/P
14	Drive select 3	I/P
16	Pulled to +5 V via 150 Ohm	I/P
18	Pulled to +5 V via 150 Ohm	1/P
20	Step	I/P
22	Write data	I/P
24	Write gate	I/P
26	Busy/track 0	0/P
28	Write protect	0/P
30	Read data	0/P
32	Pulled to +5 V via 150 Ohm	I/P
34	No connection	0/P

Pins: 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31 and 33 are all at 0 V.

SCSI

Pin	Function	Pin	Function
1	0V	2	Data bus bit 0 (LSB)
3	0V	4	Data bus bit 1
5	0V	6	Data bus bit 2
7	0V	8	Data bus bit 3
9	0V	10	Data bus bit 4
11	0V	12	Data bus bit 5
13	0V	14	Data bus bit 6
15	0V	16	Data bus bit 7 (MSB)
17	0V	18	Data bus parity
19	0V	20	Ground
21	0V	22	Ground
23	0V	24	Ground
25	open	26	Terminator power (+5 V)
27	0V	28	Ground
29	0V	30	Ground
31	0V	32	Attention
33	0V	34	Ground
35	0V	36	Busy
37	0V	38	Acknowledge
39	0V	40	Reset
41	0V	42	Message
43	0V	44	Select
45	0V	46	Control/Data
47	0V	48	Request
49	0V	50	Input/Output

SCSI interface connector: 50 way, 2 row, 0.1 inch pitch

Appendix G Mechanical specification and standards

Hardware features

Main computer unit

Dimensions

Overall height:	120 mm
Overall width:	480 mm
Overall depth:	406 mm

Colour

Pearl white-ral 1013 - metal work
Pantone warm gray 3 - submoulding

Finish

Mouldings - light spark
Metal work - painted to match light spark finish of mouldings
Rear metal work - smooth finish

Materials

Plastic - ABS, flame retardant, approved to IEC 950

Packaging

Plain brown carton:	300/300 cardboard
Lower packaging:	Etherfoam/neopolene
Upper packaging:	Expanded polystyrene

Keyboard

Dimensions

Width:	485 mm approximately
Depth:	205 mm approximately
Height:	46 mm flat - raised to 65 mm including feet

Colour

Pearl white - Ral 1013 - case
Pantone warm gray 3 - keytops
Pantone warm gray 6 - keytops

Finish

Light spark mouldings

Materials

Case:	Plastic - ABS, flame retardant, approved to IEC 950
Function key holder:	Methyl-methacrylate (perspex)

Packaging

As part of the main computer unit.

External storage unit

Dimensions

Overall height:	120 mm
Overall width:	260 mm
Overall depth:	406 mm

Colour
Pearl white-Ral 1013 - metal work

Finish
To match main unit

Weight
7:5 kilos

Packaging

Outer carton:	300/300 cardboard
Lower packaging:	Etherfoam/neopolene
Upper tray:	Expanded polystyrene

Monitor

Colour
To match main computer unit.

External cables

Cable	Acorn part number
IEC mains cable assembly	0174,727
BNC cable assembly	0174,731
SCSI (0.4M) delta cable specification	0174,734
SCSI (1.2M) delta cable specification	0174,790
Parallel printer cable specification	0174,791
Laser printer cable specification	0173,741
IEC male to female mains cable	0870,355
BNC to BNC 75R 1.0 m cable	0870,706

Safety

This section applies to all equipment in the system.

Electrical safety

The equipment meets the EEC low voltage directive for electrical equipment.

The product is designed, manufactured and tested to comply with the following standards:

- BS 415 (IEC 65)
- BS 5850 (IEC 380)
- IEC 950.

Interference generation

The product is designed, manufactured and tested to comply with the following standards:

- BS 6527 (class A)
- VDE 0871 (class A).

Interference susceptibility

The equipment will perform fully to specification under the following conditions:

Mains borne interference
Voltage spikes of peak amplitude 1000 V, positive and negative polarity, with a rise time of 5 ns and duration 100 ns. Spikes will be non-synchronous with the mains input and have a frequency of 0.2 times the mains frequency. They will be both symmetrically and asymmetrically coupled. (A generator complying with the above features is the Schaffner NSG 22A.)

Mains line disturbances
Input supply voltage with reductions as follows:

Input Voltage	Duration	Repetition Rate
0 V	20 ms	2s
50% of nominal	50 ms	2 **s**

Static discharge
When tested with a static discharge simulator complying with the proposed standard IEC 65 which specifies 150 Ohm and 150 pF human body model, the following limits apply:

5 kV - soft error self-recoverable at keyboard

15 kV - catastrophic failure.

Environmental

Temperature		
	Operational	10 to 35 deg C
	Non-operational	-30 deg C to 60 deg C
Humidity		
	Operational	20 to 90% RH (non-condensing)
	Non-operational	10 to 90% RH (non-condensing)
Altitude		
	Operational	Up to 2,500 m above sea level
	Non-operational	Up to 10,000 m above sea level
Mechanical Shock		
	Non-operational	Being tilted about each of the bottom edges to a height of 100 mm or 30 degrees with the horizontal (whichever is least severe) and then dropped three times from each corner. Three parallel falls from a height of 100 mm. Three impacts of 0.5 N on each accessible face.
	Shipment and storage	Capable of withstanding one drop on each face, corner or edge without damage to equipment or undue damage to the packing from a height of one metre (subject to the minimum capability of bought-in units ie monitor and laser beam printer).
Vibration		
	Non-operational	Random vibration to BS2011, Pt 2.1 Test Fd with the following parameters: 20-2000 Hz, 0. 0005 g2/Hz, hours total, two hours in each perpendicular plane.

Thermal Shock

Non-operational	+70 degC to -30 degC (repeated 3 times). Proc. 0980.530.

Hardware reliability

Operational lifetime

The expected operational lifetime of the equipment is 50,000 hours.

Reliability

The expected mean time between failures at which time the system may be simply repaired in order to achieve the operational lifetime is: greater than 10,000 hours.

Floppy disc
The soft read error (ie detectable and correctable on retry) rate for the floppy disc is less than one bit error per 10^9 bits.

The hard read error rate (ie detectable but not correctable) for the floppy disc is less than one bit error per 10^{12} bits.

The seek error rate is less than one seek error per 10^6 seeks.

Winchester disc
The soft read error (ie detectable and correctable on retry) rate for the Winchester hard disc is less than one bit error per 10^{10} bits.

The hard read error rate (ie detectable but not correctable) for the Winchester is less than one bit error per 10^{12} bits.

The seek error rate is less than one seek error per 10^6 seeks.

Streaming tape cartridge drive (internal)
The error rate is better than one bit in 10^{14} (with ECC in use).

Monitor
The expected mean time before failure is: greater than 20,000 hours.

Maintenance

The following operations may need to be carried out by the user:

- replacement of batteries (every year)
- cleaning of mouse rollers, replacing printer toner cartridge (as required) and changing filters (as required)
- Cleaning the head and capstan of the streaming tape cartridge drive, as required.

Warranty

The warranty period is 12 months from the date the customer receives the equipment. The warranty cover provides on-site eight hour working response. Chargeable service and maintenance contracts are available.

Appendix H Bibliography

1. Acorn Computers Ltd

2. IOC Data Sheet
   Acorn Computers Ltd

3. VIDC Data Sheet
   Acorn Computers Ltd

4. MEMC Data Sheet
   Acorn Computers Ltd

5. ANSI Small Computer Systems Interface Specification X3.131 - 1986

6. The Ethernet LAN
   Data Link Layer and Physical Layer Specification
   Version 1 (The 'Blue Book')
   Published by:
   The Xerox Corporation

7. ANSI/IEEE Std 802.3
   Local Area Network Standard
   Carrier Sense, Multiple Access with Collision Detection
   Published by:
   The Institute of Electrical and Electronic Engineers Inc.
   Distributed by:
   Wiley-Interscience

8. CSMA/CD Local Area Networks
   Part 2 Guide for implementors
   Published by:
   British Standards Institute
   2 Park Street
   London
   W1A 2BS
   Order code: DD 98 Part 2

9. Microcommunications Handbook
   LAN Components User's Manual
   Published by:
   Intel Literature Sales
   PO Box 58130
   Santa Clara
   CA 95052-8130
   Order number: 231658-002

10. Ethernet Podule Product Specification
Published by:
Acorn Computers Ltd.
Reference code: 0373,000/PS

11. Acorn Technical Publishing System User Guide
Acorn Computers Limited
Part Number 0474,901

12. Acorn Technical Publishing System Programmer's Reference Manual
Acorn Computers Limited
Part Number 0474,904

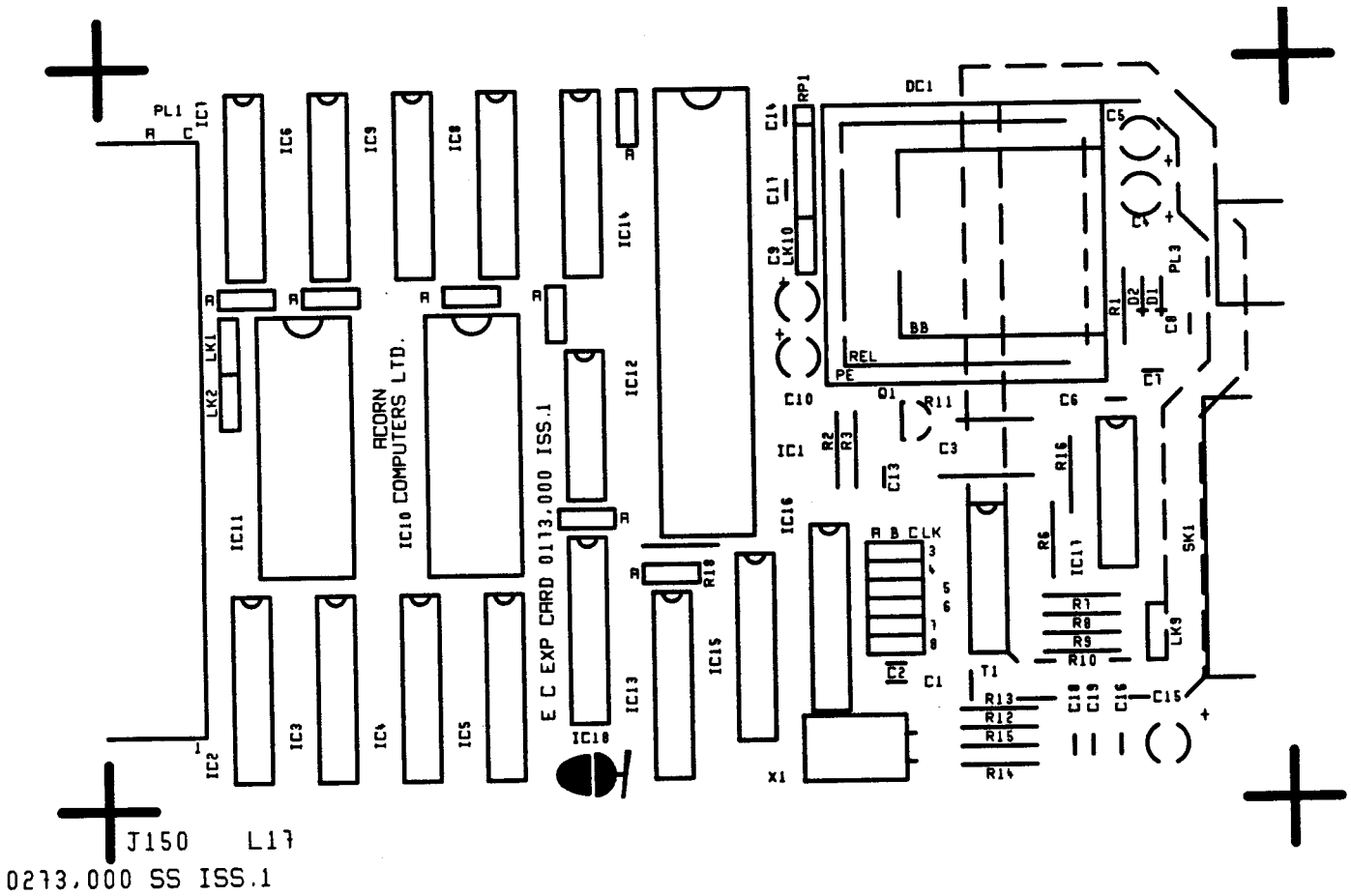
13. Acorn Technical Publishing System Service Manual
Acorn Computers Limited
Part Number 0474,900

Appendix I Silk-Screen diagrams

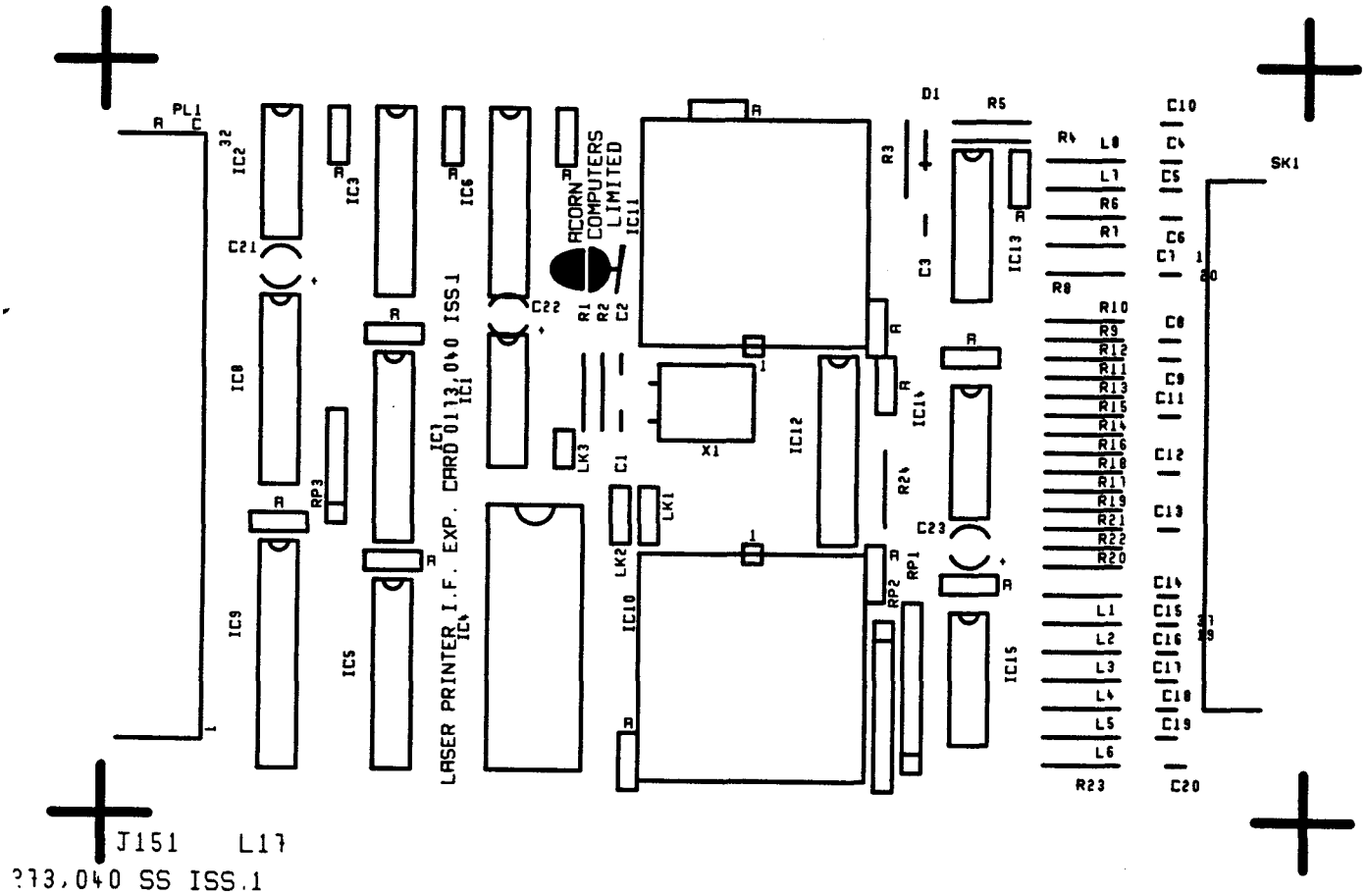
The Silk-Screen diagrams in this appendix are:

- The Main Printed Circuit Board
- The Ethernet/Cheapernet Podule
- The Laser Printer Interface Podule
- The Streamer Tape Controller Podule
- The 4 way Backplane

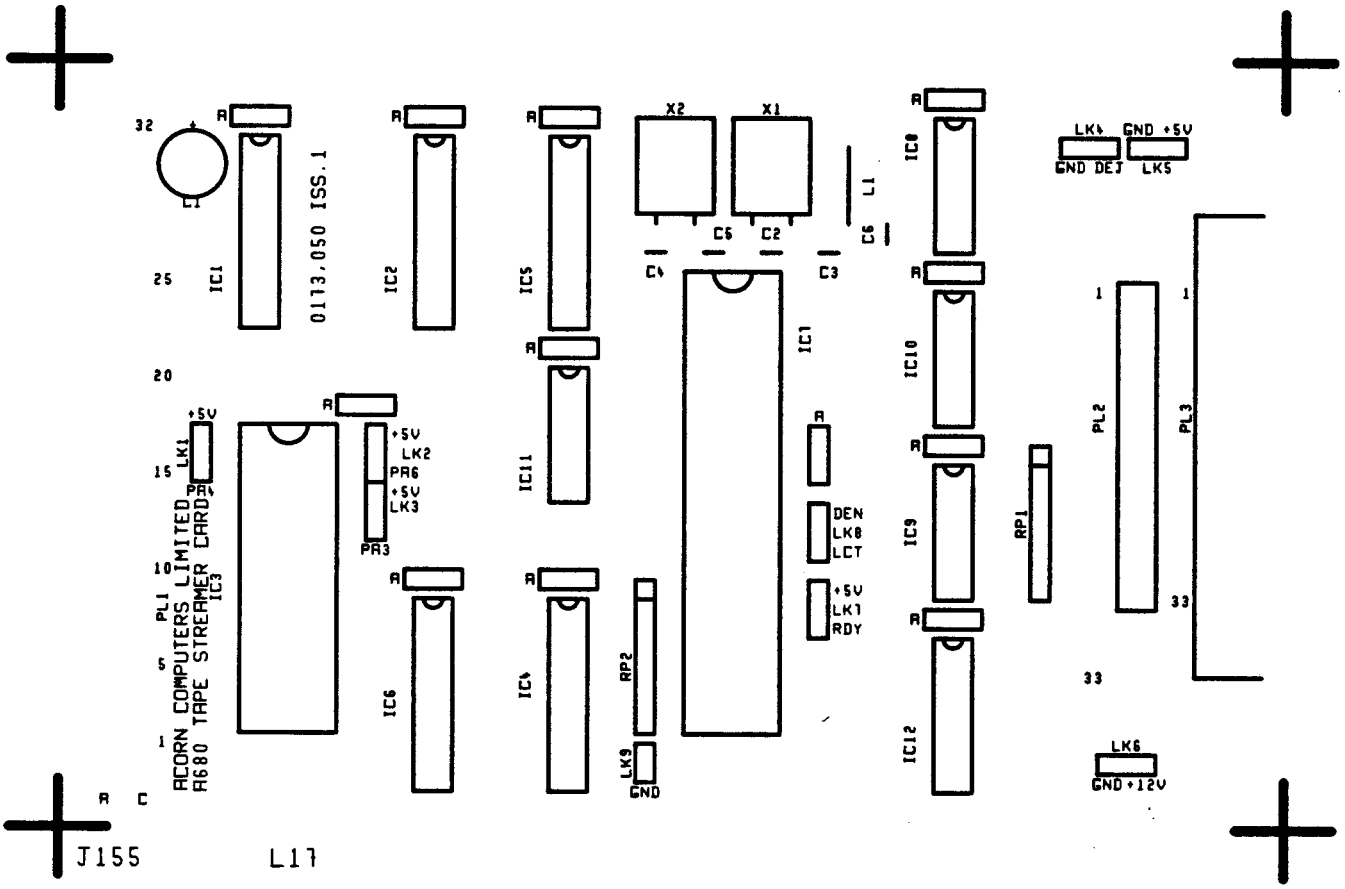
The Ethernet/Cheapernet Podule



The Laser Printer Interface Podule



The Streamer Tape Controller Podule



The 4-Way Backplane