Risc PC
CPU Bus Interface
Functional Specification

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Contents:

1: Introduction

Risc PC is the first of Acorn's 32 Bit ARM based platforms to offer support for more than one bus master. This typically allows a 2nd CPU to be connected to the system, whilst sharing resources (such as memory & I/O) with the native CPU. A set of ARM data, address and control signals are provided for this purpose on the Processor Bus (PBus). Physical connection is via two 96 way DIN socket connectors on the Risc PC motherboard, of which one must contain the native ARM CPU. It is expected that future platforms other than Risc pc will provide a PBus connection, although they may well only provide one socket if the native ARM CPU is fitted to the main PCB.

The PBus allows two bus masters to co-exist and pass control of the bus between each other. They may both access main memory and memory mapped 10. However, both cards must conform to the PBus timing spec, which is essentially the same as that of the ARM processor. The operation of the bus is described in this Functional Specification. However, for detailed timing information, the reader is referred to the ARM610/700 and IOMD data sheets. At least one card must contain an ARM CPU and at least one ARM card will be directly connected to the memory system - the native or 'host' ARM card. The 2nd card is then required to contain all necessary arbitration logic.

For example, the 2nd bus master may be another ARM to provide a degree of parallel computation, or a 2nd ARM for a dedicated task, such as DSP engine, network management or graphics pre-processing. Alternatively, the 2nd bus master may be a 'foreign' CPU, such as one of the Intel 80x86 processor family. Because both cards have full access to the machine's resident memory and I/O, providing an 80x86 processor with no other 80x86 support ICs necessary allows a very cost effective and high performance DOS support system to be implemented. Other possibilities would be to utilise a true DSP processor for speech I/O or image processing, or an application specific device such as an MPEG video processor.

The 2nd PBus card must contain all necessary arbitration logic, as 'host' cards only consist of the ARM processor itself, clock generation and any co-processing IC that may be appropriate. If the 2nd CPU is not another ARM, then it will also need to convert its own bus protocol to that of the PBus (ARM protocol). Due to the critical timing of relevant signals, the recommended method for implementing such conversion circuitry is to make use of an Application Specific IC (ASIC).

Both Slot 0 and Slot 1 are functionally identical, however, it is recommended that, for consistency the 'host' ARM card sits in slot 0 and the 2nd bus master occupies slot 1.

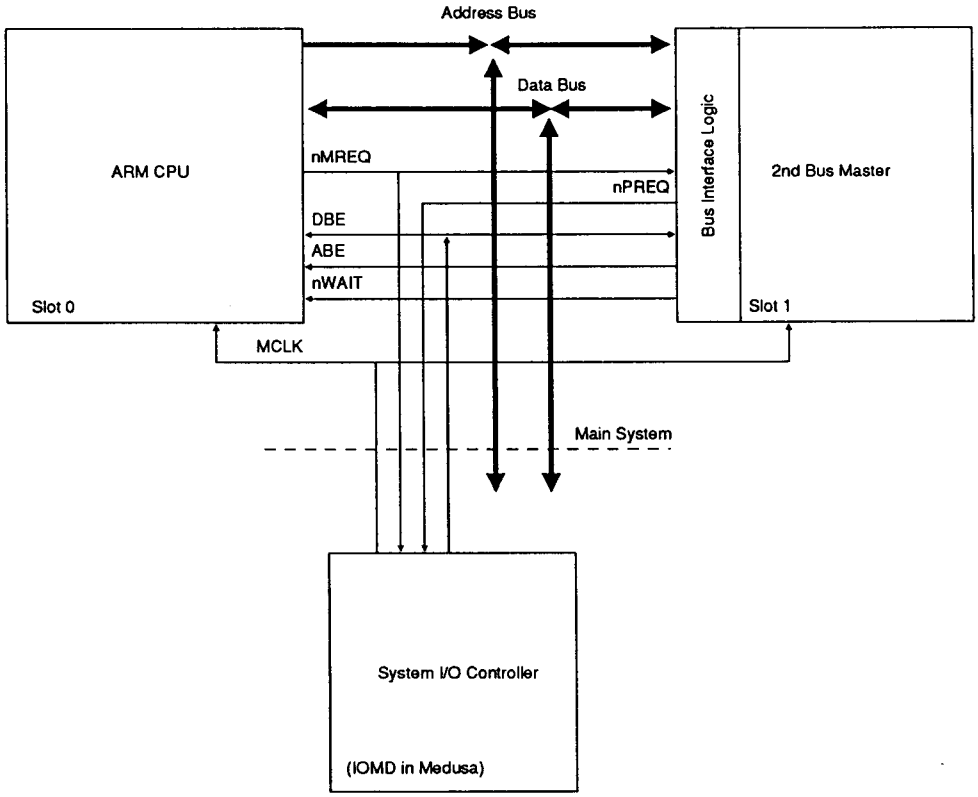
Due to space constraints within the current Risc pc case, the layout of components on each card is restricted as shown in the physical dimensions diagram overleaf. In most cases, with surface mounted ICs this will not be a problem. However, all sockets, for example will need to be mounted on the front of the card, as typically they will exceed 4.5 mm in height. A further consideration is that all devices which consume significant power should be mounted on the front of the card, as the space between the two cards for ventilation is limited. Typically, this means that the bus arbitration ASIC can be mounted on the reverse, but the 2nd bus master itself and any associated memory devices should be on the front.

All current Acorn designed 'host' ARM cards are single sided and can therefore theoretically occupy either slot. However, as stated above it is recommended for consistency that slot 0 is reserved for the 'host' ARM CPU even in a machine with only one card resident.

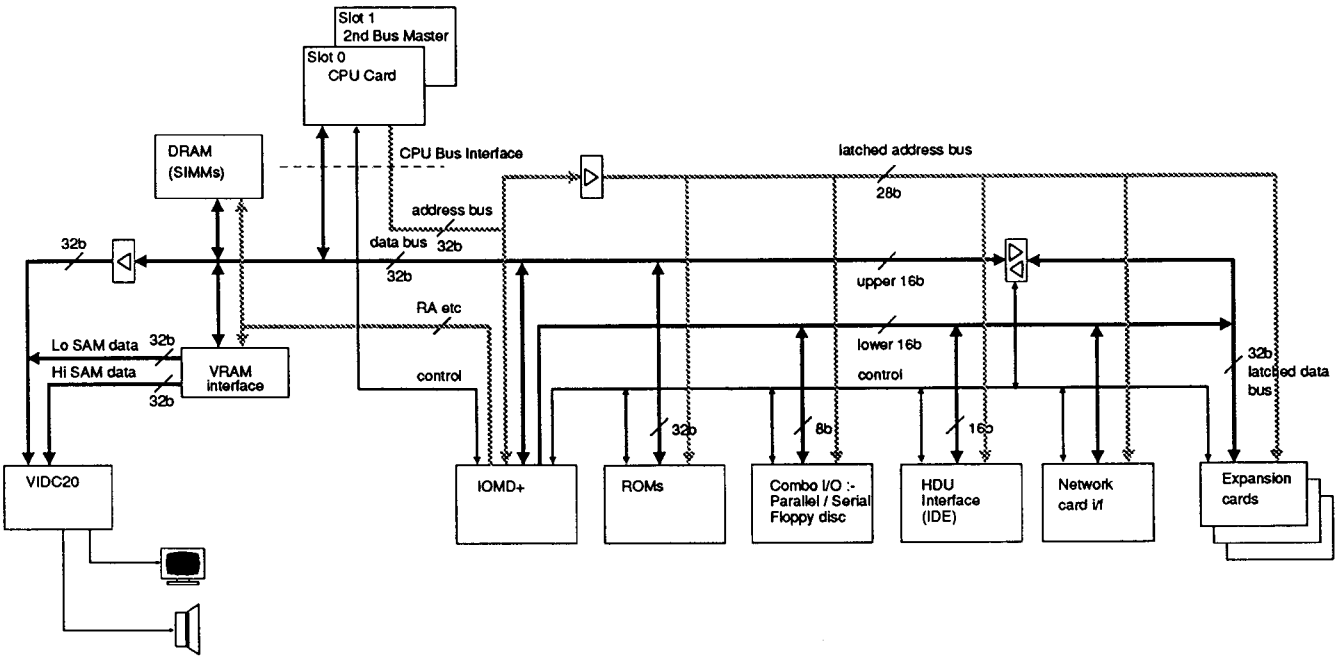
The following diagram shows how the PBus is integrated into the Risc pc system.

1:1 System Block Diagram

The block diagram below gives a graphical representation of the bus arbitration communication between the host ARM card and a 2nd Bus master.



The first implementation of the PBus interface is within the Risc pc platform, and in order to illustrate the way the bus communicates with the system as a whole, a block diagram for Risc pc is given below.



2: **Bus arbitration**

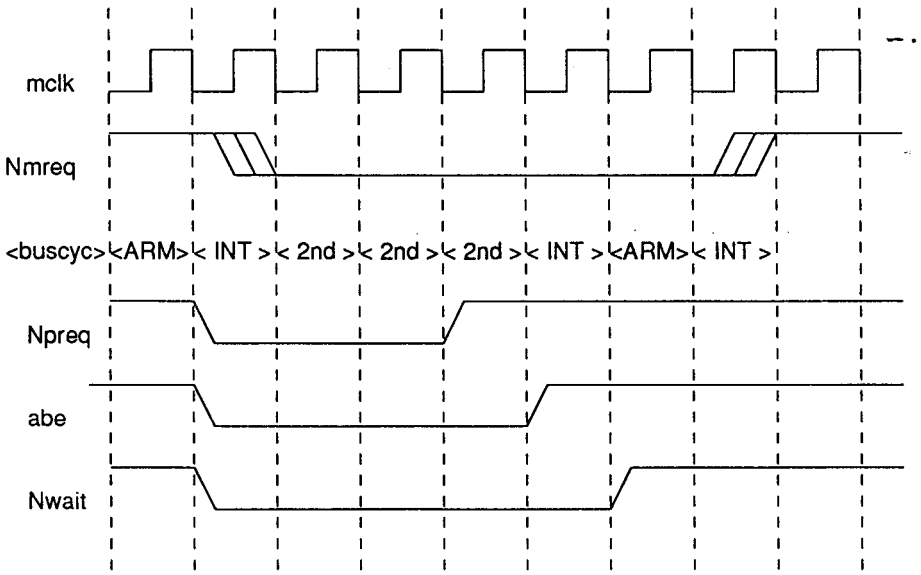
Support for a secondary bus master is provided essentially by Npreq. This signal is similar to Nmreq, but with higher priority. An interface circuit allows the second bus master to emulate an ARM bus. It is recommended that this be implemented in an ASIC. This ASIC must ensure that unaligned accesses are converted to ARM byte or word accesses, and make sequential accesses truly sequential (thus an 80486 cache line fill, for example, would have to be modified if it does not start on a quad word boundary). The interface circuit must also do all the arbitration between the second processor and the ARM, and thereby decide when to assert the Npreq signal.

The interface circuit must first wait for a safe time to commence the arbitration, stop the ARM bus clock using the Nwait pin, and then perform an access, or burst of sequential accesses. The interface circuit arbitrates in MCLK high periods, and drives registered outputs from the falling edge of Mclk.

An additional I-cycle (ie. non-memory request cycle) is inserted between the ARM and second bus master bus bursts. The second bus master can only request the bus if it sees that the ARM is about to do an internal cycle. This first internal cycle is stretched to the ARM (with Nwait) and merged with the next sequential bus cycle by the second processor with no cycle overhead, by removing ABE and driving second processor addresses onto the bus. ABE is the ARM bus enable signal, which output-enables the address and data buses, and relevant control lines. The second bus master interface must also observe the ARM LOCK signal and must not request the bus in the internal cycle between the read and write cycles of a SWAP instruction.

When the second bus master interface completes a transfer, or burst of sequential transfers, it removes it's pipelined request, and on the following cycle re-asserts the ABE signal. One cycle later still, it removes the Nwait signal to the host ARM, which is then free to continue from where it left off. When ABE is re-asserted but the ARM clock is still held by Nwait, an internal cycle is inserted for bus turnaround. This ensures correct merged internal - sequential operation, should the ARM require the bus immediately.

If the second bus master interface removes its request for only one Mclk period and then reasserts it, IOMD does not relinquish the bus to the ARM and thus 486-Locked cycles (for example) may be performed. If however more than one cycle of Npreq removal occurs then the interface must relinquish the bus and wait for an ARM entering Internal cycle condition.



In the diagram above <buscyc> indicates the bus cycle currently being executed. The diagram shows he second bus master performing a three-word burst access. The first internal cycle, shown as <INT> in the diagram is the extra internal cycle added for the bus changeover. The first second bus master cycle, shown by the <2nd> symbol would actually be the I-cycle of a merged I-S cycle, as IOMD only uses I-cycles and S-cycles. Therefore N-cycles are made from merged I-S cycles, as is done by the ARM3 CPU (prior to the ARM6) for example. Hence there is an extra I-cycle inserted by IOMD during bus change-over. The second bus master has the bus during the period indicated by <2nd> above, during this period, it is controlled by mclk.

3:1 **Signal description**

All signals shown in *italics* are Risc pc specific and will not appear on other platforms.

Name	Function	Main	ARM	2nd
A[28:0]	Address Bus. Driven by the current bus master.	I	OZ	IOZ
A[29]	Risc pc also has this address line tracked but it is not tested. [1]			
D[31:0]	Data Bus. Driven or read by the current bus master, or tri-stated during DMA operations	IOZ	IOZ	IOZ
MCLK	Memory clock. Driven by IOMD on the Main PCB motherboard	O	I	I
nR/W	not Read/Write. Driven by the current bus master. Low indicates a read cycle.	I	OZ	IOZ
nB/W	not Byte/Word. Driven by the current bus master. Low indicates to IOMD that only a byte should be written in this cycle.	I	OZ	10Z
nMREQ	not memory request. Driven low by the host ARM to indicate that it wishes to use the bus in the next cycle.	I	O	I
nPREQ	not processor request. Driven low by the 2nd bus master to indicate to IOMD that it wishes to use the bus in the next cycle. 4K7 pull-up on motherboard.	I	NC	O
DBE	Data bus enable. Driven low by IOMD during DMA. The host ARM and 2nd bus master should both tri-state their data busses when this signal is low.	O	I	I
ABE	ARM bus enable. Driven low by the 2nd bus master to tri-state the ARM's address, data and control (nR/W, nB/W and LOCK) busses. 4K7 pull-up on host ARM card.	[2]	I	O
nRESET	not reset. System reset line. Main PCB drives this low during power on or other reset.	O	I	I –.
nFIQ	not fast interrupt request. Provided only on Risc pc [3] Driven low by IOMD to indicate a fast interrupt request to the ARM.	O	I	NC
nIRQ	not interrupt request. Provided only on Risc pc [3] Driven low by IOMD to indicate an interrupt request to the host ARM.	O	I	NC
nWAIT	not wait. The 2nd bus master drives nWAIT low to stall the host ARM whilst it is active. 4K7 pull-up on host ARM card.	[2]	I	O
LOCK	Locked operation. Driven high by the host ARM when executing a SWP instruction to indicate a locked memory cycle.	[2]	O	I
nPirq	not Podule interrupt. Driven low by the 2nd bus master to interrupt the ARM. [4] Open collector. 4K7 pull-up on motherboard	I	NC	OD
nPfiq	not Podule fast interrupt. Driven low by the 2nd CPU to interrupt the ARM. [4] Open collector 4K7 pull-up on motherboard	I	NC	OD
RCLK	Reference clock. A less stretched version of MCLK provided by IOMD. Present only on the Risc pc PCB, Untested and missing in future platforms.	O	NC	[5]

All signals are TTL input threshold, unless otherwise stated
Key: Main Risc pc main PCB motherboard

ARM Host ARM card

2nd	Second bus master
	Input
O	Output
Z	Signal can be tri-stated
NC	For this card, it is expected that this signal will not be connected as it is of no obvious use.
OD	Output - Open Drain

Notes:

1 A[29] is tracked between the connectors on the motherboard and is fed into the system address latch, but not used. A 2nd bus master card should not use this signal as it is untested and may be removed

2 ABE, nWAIT and LOCK signals are tracked between the connectors on the motherboard, but are not connected elsewhere on the Risc pc motherboard.

3 The signals nFIQ and nIRQ are provided because in Risc pc, the native ARM CPU is connected to the system via a 'host' PBus card. The host ARM must have interrupt access to the system controller IOMD on Risc pc, on platforms where the host ARM processor is fitted to the motherboard and only one PBus socket is provided solely for a 2nd bus master these signals will be missing.

4 The use of the podule bus interrupt lines allows easy software integration for 2nd bus master interrupt servicing. An interrupt flag register must be present in the bus interface ASIC to allow the system to identify whether the interrupt was generated by a podule, or the 2nd bus master. An interrupt mask register must also be provided. In addition, a global mask register in IOMD may be used to disable all podule interrupts.

5 On Risc pc, the RCLK signal is provided as an input to the 2nd bus master card. However, it will not be provided on other platforms, and so a 2nd bus master card must work without this signal.

For detailed signal timing information - such as set up time from MREQ - please refer to the ARM 610/700 and IOMD data sheets.

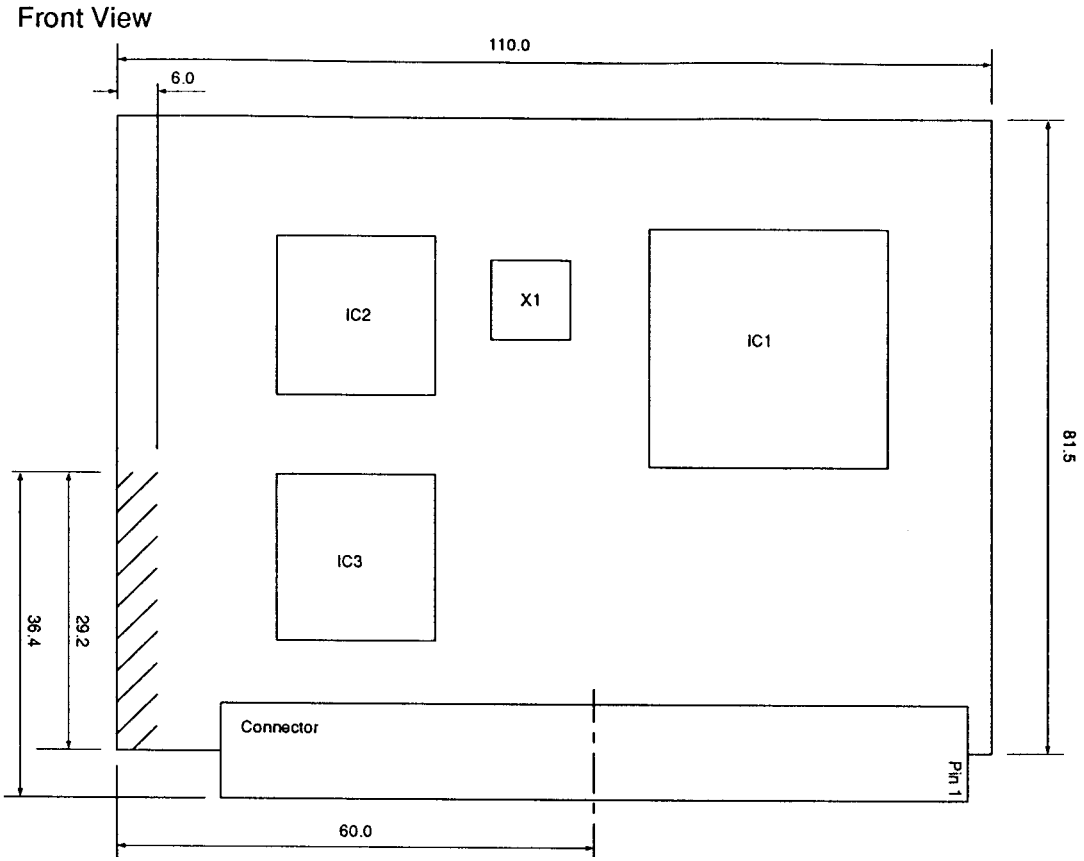
3:2 PBus connector pinout

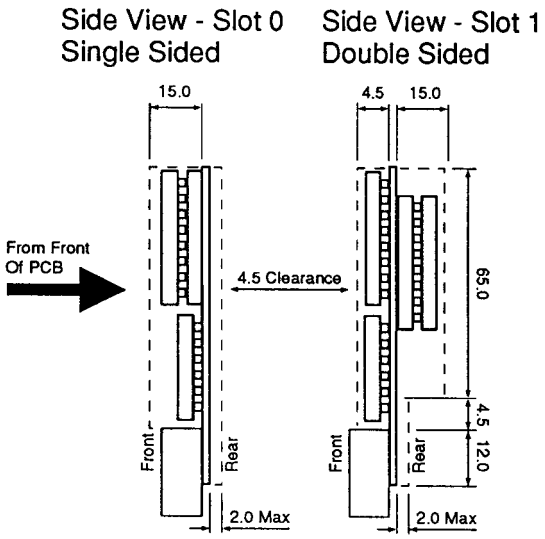
Connector Row

Pin	A	B	C
1	0V	D[0]	D[1]
2	D[2]	D[3]	D[4]
3	D[5]	D[6]	D[7]
4	D[8]	D[9]	0V
5	D[10]	D[11]	D[12]
6	+5V	D[13]	D[14]
7	D[15]	D[16]	D[17]
8	D[18]	0V	D[19]
9	D[20]	D[21]	D[22]
10	D[23]	D[24]	D[25]
11	D[26]	D[27]	D[28]
12	D[29]	D[30]	D[31]
13	DBE	*Tck*	nMREQ
14	0V	*nIRQ*	0V
15	*nFIQ*	nPREQ	*Trst*
16	+5V	n RESET	*Tms*
17	nPFIQ	nPIRQ	*RCLK*
18	ABE	0V	nR/W
19	nB/W	LOCK	*Tdol*
20	nWAIT	*Tdi*	MCLK
21	A[0]	A[1]	A[2]
22	A[3]	A[4]	A[5]
23	A[6]	A[7]	A[8]
24	A[9]	A[10]	0V
25	A[11]	A(12]	A[13]
26	+5V	A[14]	A[15]
27	A[16]	A[17]	A[18]
28	A[19]	0V	A[20]
29	A[21]	A[22]	A[23]
30	A[24]	A[25]	A[26]
31	A[27]	A[28]	*A(29]*
32	OV	*Tdo2*	0V

Note: The signals *Tck, Trst, Tms, Tdi, Tdol & Tdo2* are reserved for boundary scan test signals.
Tdo1 test output of the first device.
Tdo2 test output if two boundary scan devices are fitted onto card.

3:3 Physical Dimensions and Pin Orientation





All dimensions in mm
Tolerances: ± 0.2 unless specified
The number & orientation of ICs on this diagram is for guidance only

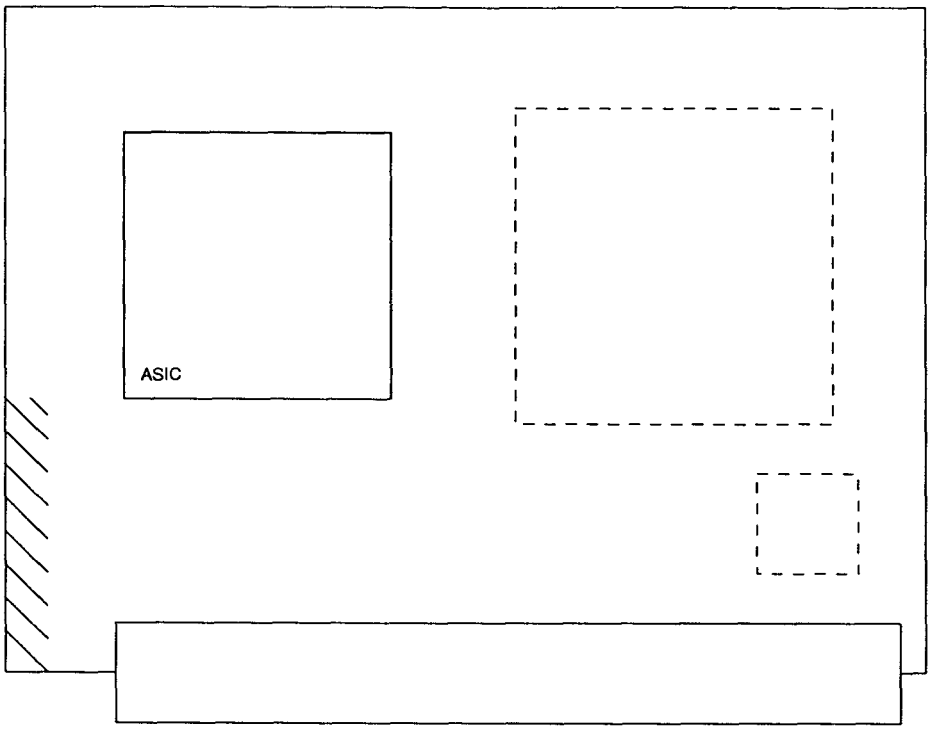
NOTE 1: No components or copper to encroach into hatched area
NOTE 2: Connector is a standard 96 way right angle DIN 41462 plug
NOTE 3: Only low power dissipation devices may be fitted on front of slot 1 card
NOTE 4: Board Thickness: 1.6mm

The following two diagrams give suggested physical layouts for both an 80486SX 2nd PBus card and an 80486DX based 2nd PBus card. The two options allow an upgrade route to 80487 floating point co-processor, or 82495DX based secondary cache respectively. These layouts obey the above height constraints and ensure adequate space for ventilation.

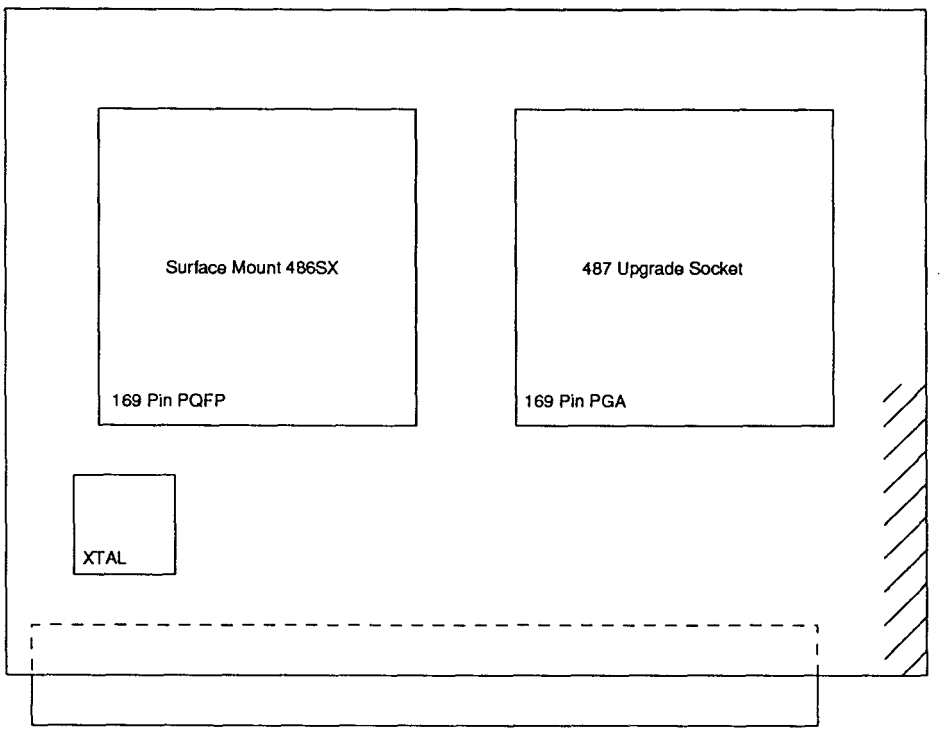
The diagrams are to scale and are intended to show space allowances only

3:3:1 80486 2nd PBus card examples - 486SX based with 487 upgrade socket

Front View



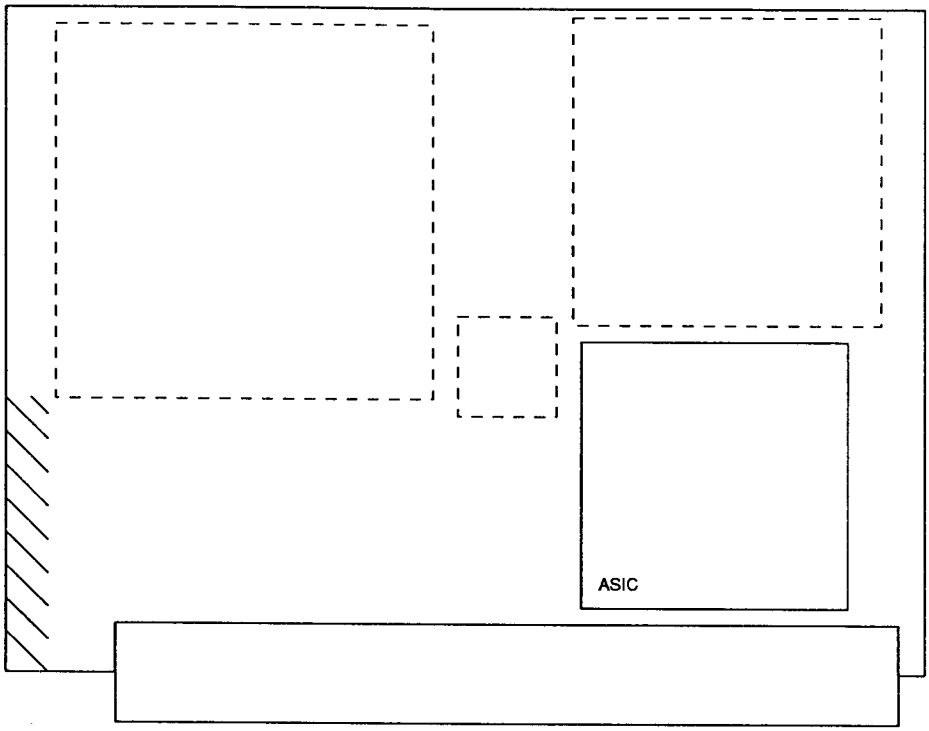
Rear View



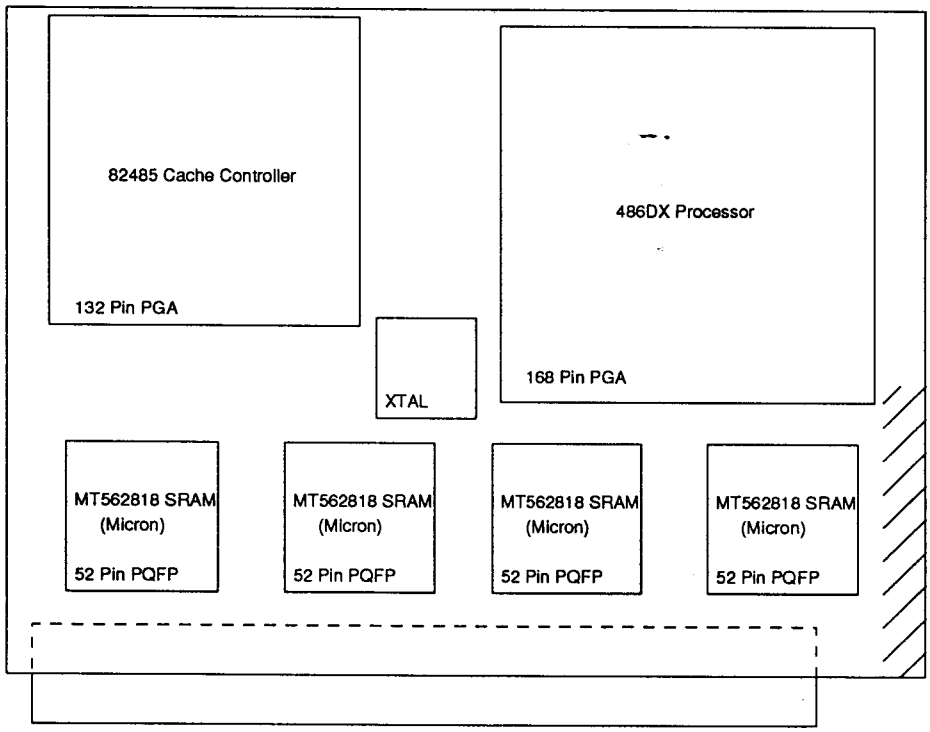
Both views drawn to scale

3:3:2 80486 2nd PBus card examples - 486DX based with secondary cache

Front View



Rear View



Both views drawn to scale

4: Capacitive Loading

Address Bus	max	20	pF
Data Bus I/O	max	20	pF
Control signals	max	20	pF

4:1: Drive Capability

Address Bus	min	80	pF
Data Bus I/O	min	200	pF
Control signals	min	80	pF

5. Power Consumption Allowance

The host ARM CPU cards should consume no more 500 mA at (5.0 ± 10%) V

The 2nd bus master card should consume no more than 1.5A at (5.0 ± 10%) V