A1	DRG. No. 0186,000 /C	FIRST USED ON	THIRD ANGLE PROJECTION	IF IN DOUBT ASK	DO NOT SCALE

HF Decoupling

Bulk Decoupling

Cont. on Sheet 4

Track Width 35

Power On LED LK14

MSV Track Width 35

6WPowerPLG PL5

INPUT POWER SOCKET

PL9 PL8 PL7 PL6

From Sheet 2

From Sheet 3

To Sheet 3

Processor Module

PL3

R96WAYDINPLUG

X4 72.00MHz

IC39 SOCKET=SUPA 0286,023

IC4 ACT174

IC3

IC2

IC72 ACT74

IC71 SOCKET=SUPA 0286,020

IC59 AC00

IC60 MEMC1a 12MHz

SOCKET=NORM

To RAM Expansion

SK5 SK6 SK7 96WAYDINSKT

To RAM Expansion Slots

IC69 IC68 IC67 HCS73

LK4 Test Connector

IC47 IC48 IC49 IC50 ROM/EPROM

SOCKET=SUPA

RISC OS 2.01 ROM1 0270601

RISC OS 2.01 ROM2 0270602

RISC OS 2.01 ROM3 0270603

RISC OS 2.01 ROM4 0270604

ROM Size

ROM Size selection

SIZE (BITs)	LK24	LK23	LK26
512K	0	0	0
1M	1	0	0
2M	0	1	0
4M	1	1	0
8M	0	0	1

ROM Type

LK27 LK25 Tracked as 2X2

ROM Type selection

SIZE (BITs)	LK27	LK25
512K EPROM	1;2	1;2
NON JEDEC 1M ROMs	1;2	1;2
NON JEDEC 1M EPROMs	1;2	1;2
JEDEC 1/2/4/8M EPROM/ROMs	2;3	2;3

Spare Gates

IC56 IC72

To Sheet 4

To Sheet 2,3 & 4

To Sheet 3

Power and Ground Table

See Separate Sheet

ISS	DATE	DESC. OF CHANGE	ENG.	CHKD.
1	5/6/90	AMR 2495	RK	
	15/5/90	Tidy up, MClk=12MHz	RK/PW	
	1/5/90	PAL Changes	RK/PW	
1L	5/4/90	Signal Conditioning	RK/PW	
	5/3/90	Add BOT Properties	RK/PW	
C	26/2/90	Design Mods	RK/PW	
	2/2/90	Add BOT Properties	RK/PW	
	24/1/90	NF Links, add BNCs Fastons and Dcplrs	RK/PW	
	5/1/90	M.C.PLL, Test Conn & Lib./PL Updates	RK/PW	
	9/11/89	Design Review	RK/PW	
	3/11/89	Sync Changes	RK/PW	
	27/10/89	CPU & RAM Card Pinout Mods.	RK/PW	
B	18/10/89	16MByte Mods.	RK/PW	
	16/10/89	RFI	RK/PW	
	28/9/89	Checked		RK/PW
	25/9/89	Tidy Up	RK/PW	
	18/9/89	Development	RK/PW	
A	14/9/89	Development	RK/PW	

SCALE		ALL DIMENSIONS IN mm UNLESS OTHERWISE STATED
MATERIAL		
FINISH		
WHOLE No. TOL.	DECIMAL No. TOL.	ANGLE TOL.

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TITLE

MAIN PCB CIRCUIT DIAGRAM

MemC, ROM, ARM Interface Sheet 1/5

ACORN COMPUTERS Ltd | A1 | DRG.No 0185,000 /C