ACORN COMPUTERS LIMITED - PRESS RELEASE

ACORN COMPUTERS ANNOUNCE THE AVAILABILITY OF AN EVALUATION SYSTEM FOR THEIR SINGLE CHIP, 32-BIT REDUCED INSTRUCTION SET COMPUTER - THE ARM

CAMBRIDGE, UK. — 7/7/86 — Acorn Computers Ltd are making available an evaluation system for their RISC architecture CPU, the Acorn RISC Machine (ARM), first announced in August last year. This marks the first opportunity for independent developers and researchers to gain experience with this very high performance processor. Acorn Computers is producing two versions of the evaluation system, one to be used with their BBC and Master Series micros, the other to be used with IBM PC's, AT's and compatibles. The evaluation systems combine a hardware system with a comprehensive kit of software including five high level languages, a powerful Assembler and associated software tools.

The ARM's high performance processing capability is essentially derived from its ability to use a high memory band-width and its applicability is increased through its good interrupt handling. With prices being considerably less than other processors of equivalent power, the ARM offers exceptional price performance for a wide range of applications. Typical applications include communications, microcomputers, expert systems and such embedded systems as laser printer controllers, network controllers and graphics engines.

Acorn recently reached an agreement, with VLSI Technology Incorporated of Phoenix, Arizona, to manufacture and market the chip set consisting of the ARM and a series of associated controller chips. This agreement includes the establishment of the provision for a second source for the chip set.

The development of the ARM demonstrates Acorn's continued commitment to maintaining its renowned high technology expertise. "We are very excited by the opportunities that Acorn's RISC technology has created", commented Brian Long, Managing Director of Acorn. "The chips are being made available as an

open system so that the technology can be implemented across **a** wide range of applications and a number of major companies, including Olivetti, have already expressed their enthusiasm to carry out evaluations. Acorn will obviously be using RISC technology in certain future products."

The ARM is fabricated in low-power-consuming CMOS and offers an average execution rate of 4 Million Instructions Per Second (MIPS) using a two phase 8 megahertz clock. The ARM has only 44 basic instructions and these have been designed in such a way that efficient code which executes very quickly is produced. The ARM contains 25 32-bit registers, which partially overlap. This overlapping allows fast interrupts to occur without incurring the time-consuming task of storing the contents of the register array. The ARM is optimised for low interrupt latency and support of high-level languages.

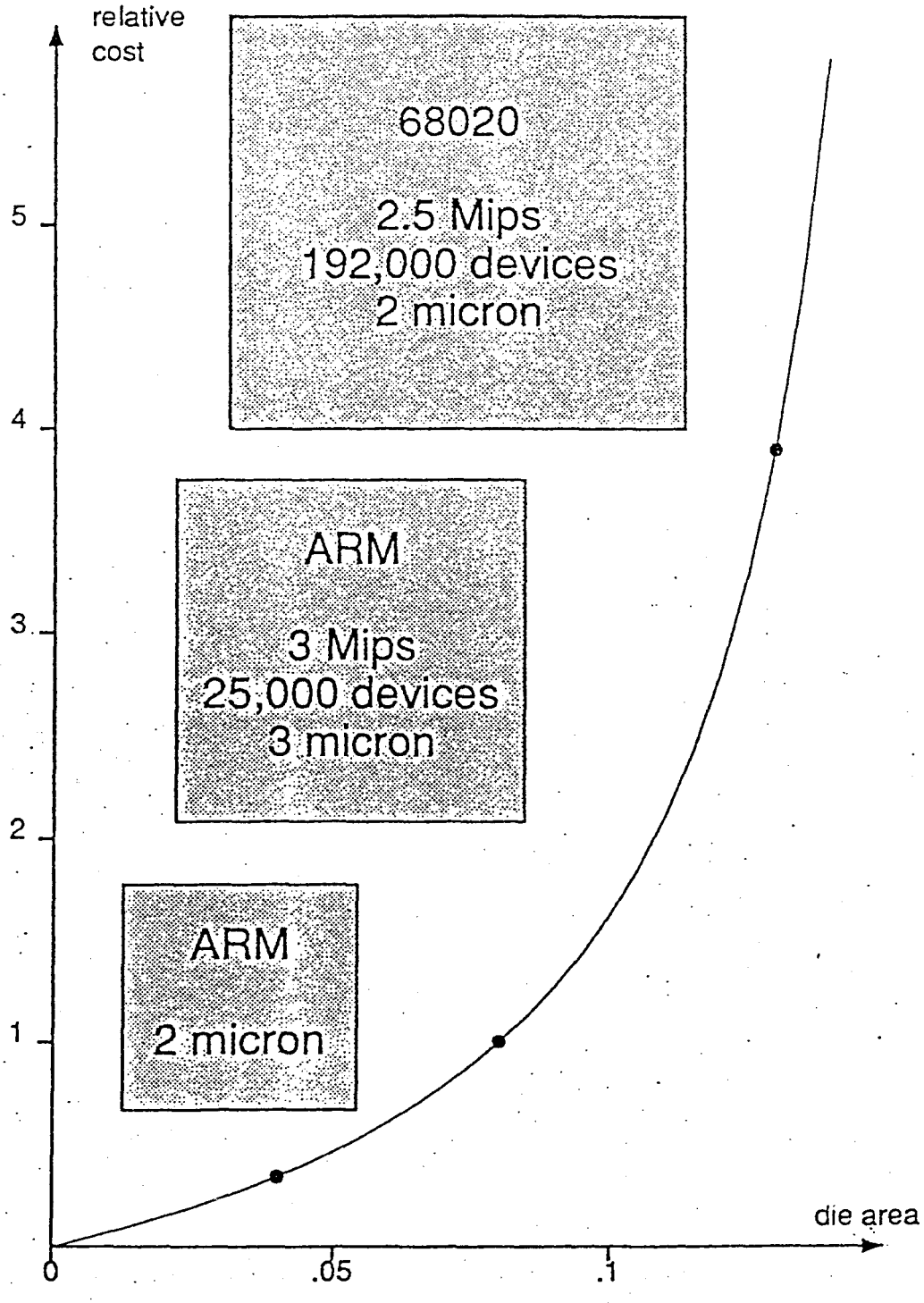
The ARM Evaluation System is available immediately at a cost £4,500 (ex. VAT). The PC ARM Evaluation System will be made available in the fourth quarter of 1986 at a comparable price.

For further information on the Evaluation Systems please contact

Bob Antell (ARM Systems Sales Account Manager)
Acorn Computers Limited
Fulbourn Road
Cherry Hinton
Cambridge CB 1 4JN

Telephone 0223 245200
Telex 817875 ACORN G

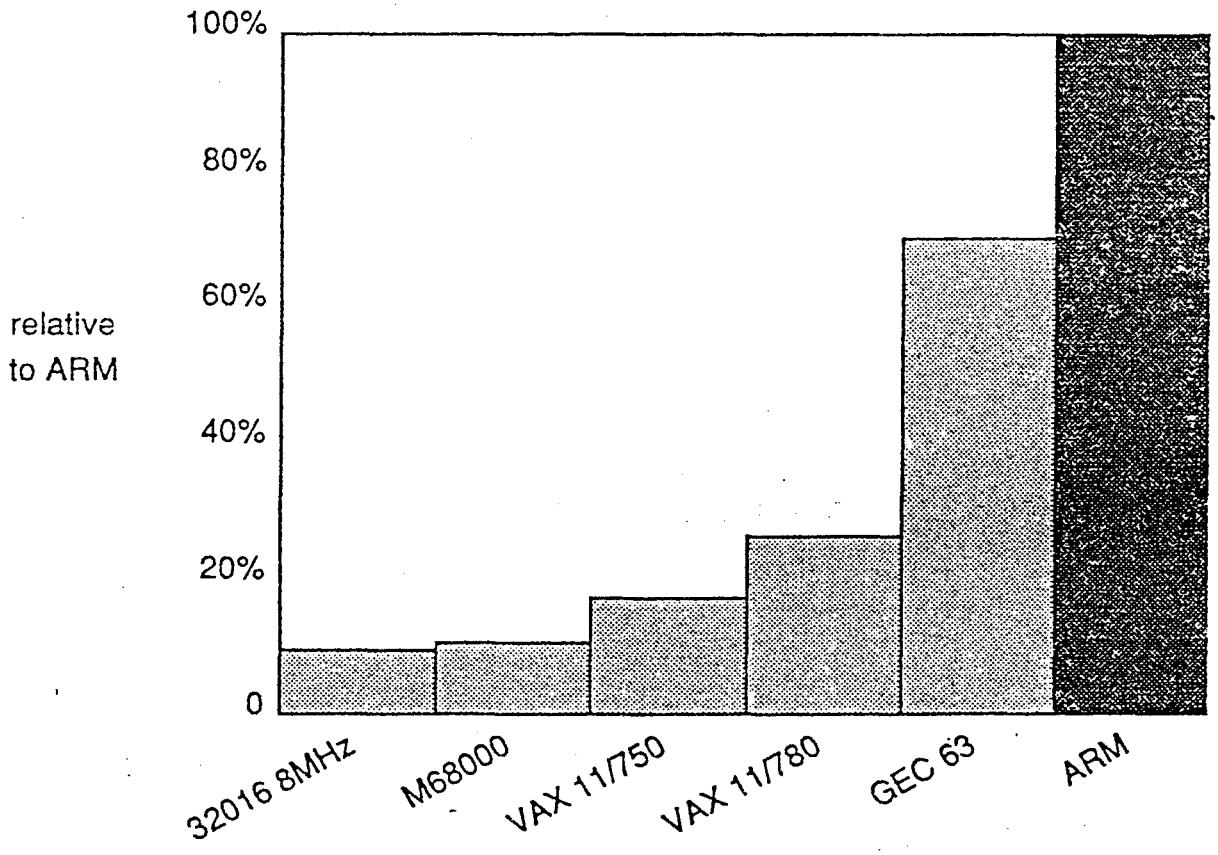
Die size vs. cost



Acorn RISC Machine

Processor chip comparisons

LISP benchmarks



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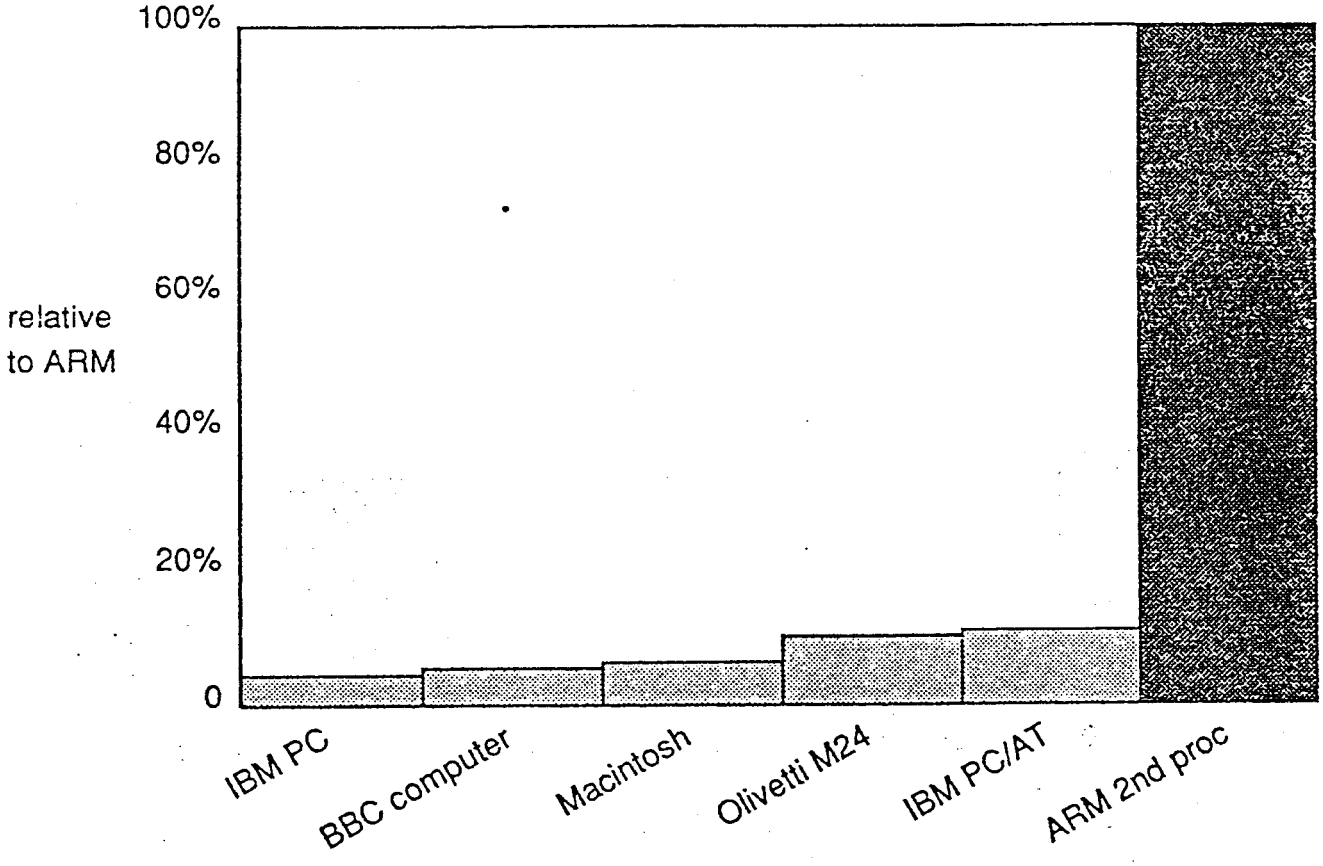
PCW Benchmarks for interpreted Basic



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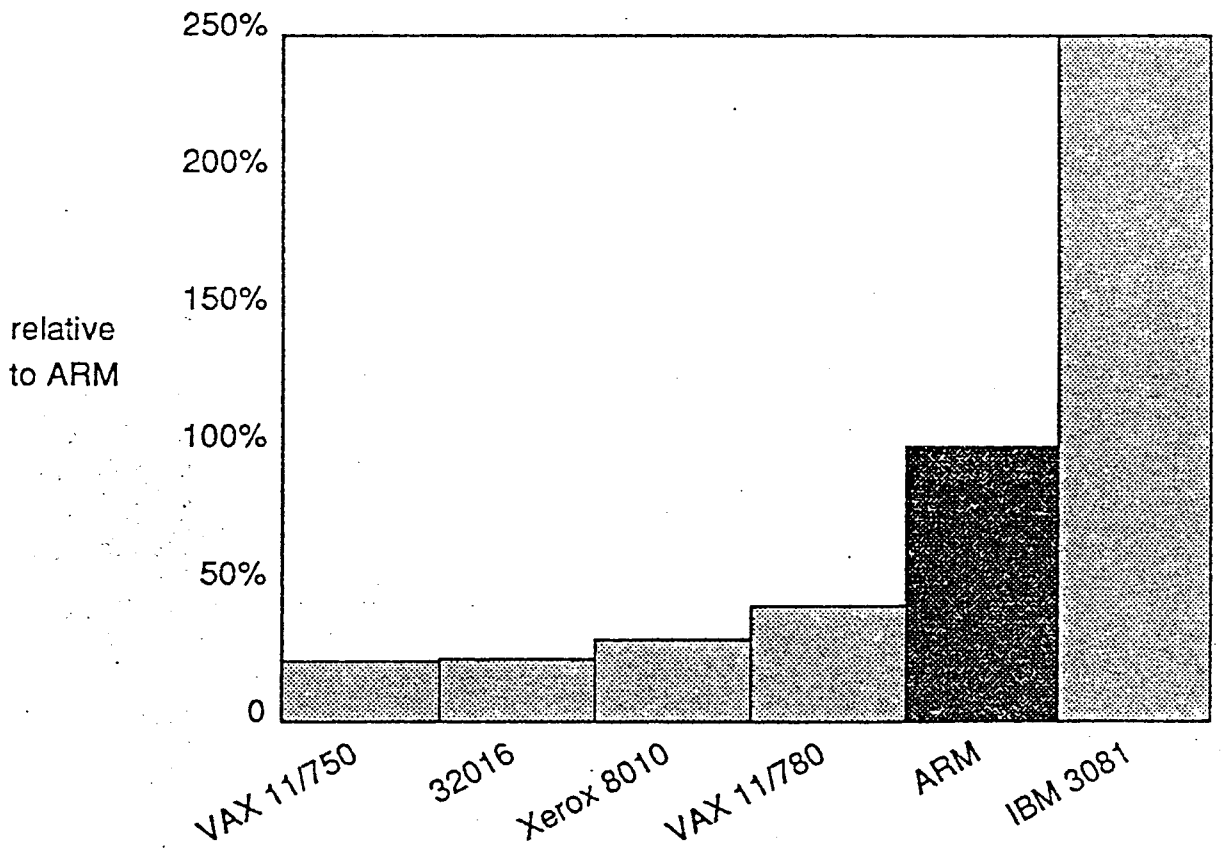
Richards' benchmark – compiled "systems" code



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USER'S OWN BENCHMARKS

Language	Nature of Benchmark	Alternative Processor	Time Secs	ARM 3um
LISP, (REDUCE)	Algebraic	VAX 11/750	280	42
PROLOG	Quicksort, 50 integers	GEC-63	0.83	0.26
BASIC	PCW BM8	BBC B	59	1.28
BASIC	PCW BM8	B+ 32016	11.8	1.28
LISP			Relative	Time
	(List only Cddr + Tak + Gtak + My Reverse)/4	VAX 11/750	1	0.18
		Symbolics 3670	0.38	0.18
		Acorn 32016	1.56	0.18
"C"	Dhrystone		Dhrystones /	sec
		Sun 3/180	3846	4995
		VAX 11/785	2146	4995
		CRAY-X-MP48	17857	4995