ARM3 Upgrade
Fitting and Operating Instructions

WARNING - Both the Archimedes and the ARM 3 upgrade are static sensitive. Exercise all possible anti-static precautions whilst fitting the upgrade: static damage is NOT covered by warranties. If your Archimedes warranty is still valid (12 months from date of purchase) then the ARM 3 Upgrade must be fitted by an approved Component Level service centre to maintain the Acorn warranty.

DISASSEMBLING THE ARCHIMEDES

- Be sure to disconnect all cables from the Archimedes case, particularly the mains power and monitor power before proceeding.
- Remove the three screws along the top of the rear of the computer and those either side of the front of the computer. Slide the top cover carefully off towards the rear.
- Remove the front fascia of the computer by unscrewing three screws along the front underside and one more on either side of the front. Unplug the fascia wiring carefully before removing it.
- If an expansion backplane is fitted then remove any expansion boards and then the backplane. Unplug the two bolts and three power connectors and then pull the back-plane firmly upwards.
- Remove the two screws which fix the diskette drive bracket onto the metal bar at the front of the computer. Take care not to lose either of the screws inside the computer. Detach the diskette power and data cables by pulling their bodies towards the rear of the computer. You should now be able to see the area of the main circuit board previously obscured by the diskette drive. Identify the large square 84-pin ARM 2 chip (it has "VL86C010" or "ARM" printed on it), and the smaller square MEMC chip (it has one or more of "MEMC", "MEMC1a" or "VL-86C110" printed on it) before proceeding further.

MEMORY CONTROLLER UPGRADE (MEMC1a)

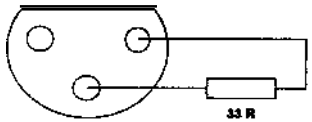
If your computer has a model number ending /1, such as 420/1, it will have a MEMC1a Memory Controller chip in it. If your computer does not contain this version of the chip, it will need to be fitted and tested before the ARM 3 upgrade. NOTE that this is NOT optional - the ARM 3 upgrade cannot operate properly without this chip.

WARNING: This upgrade must be performed by an Acorn Approved Service Centre in order not to void the warranty. T0 fit the MEMC1a upgrade you will need:

- a 68-pin PLCC chip extractor tool
- a MEMC la chip (included in kit)
- a pre-programmed PAL chip (included in kit)
- a 33 Ohm resistor (for A440 computers only, included.)

Fitting the MEMC1 a upgrade

- ON A440s ONLY: With a pair of side-cutters remove transistor Q14 from the board and then remove the three stubs of its legs from the board. This obviates the need to remove the PCB or use a desoldering tool. Form the resistor and then solder it onto the two holes as indicated in the figure:



On all models:

- Remove the MEMC from its socket using the extractor tool, noting its orientation.

Insert the new MEMC la from the kit, with the same 0rientation. Push it home with your thumb until it is flush within the socket.

- Remove the existing PAL with a screwdriver or DIP chip extractor and replace it with the one from the kit, again ensuring the same orientation.
- Reassemble and test the computer BEFORE proceeding with the ARM 3 upgrade.

INSTALLING THE ARM 3 UPGRADE

- Using an 84-pin PLCC chip extractor and NOT A SUBSTITUTE TOOL remove the ARM 2 chip from its socket. Place the chip on an anti-static surface out of the way. *SERVICE CENTRES* please note that the ARM 2 chip still belongs to the customer and you should make arrangements to hold it for them or return it to them safely packaged as they see fit.
- Remove the ARM 3 Upgrade from its packaging.
- Orient the Upgrade correctly:-
  * There is a chamfer 0n one corner 0f the plug to fit a corresponding filled-in corner in the socket.
  * The Aleph One Logo and lettering on the board should be the right way up when viewed from the front (keyboard) of the computer.
- Place the upgrade plug ON the socket and establish visually that it is correctly aligned on the socket. Using moderate force push the upgrade into the socket until you feel it click home. EXCESSIVE FORCE SHOULD NOT BE NECESSARY: examine the upgrade plug/pins and the main circuit board socket again if you feel uneasy. It will be very apparent when the plug is correctly fitted. The upgrade is quite rugged so do not be alarmed if you have to push harder than you expect. Nevertheless, the circuit board is not infinitely strong so use your common sense or you could damage it.

TESTING THE UPGRADE

- You will need to reassemble the computer, in the following order: 1) the floppy disc drive bracket (two screws) and its two cables. 2) the expansion backplane (two screws, three wires) if present. 3) the front fascia and wiring (one plug and five screws). Be careful to ensure correct alignment of the floppy disc drive as you do so - inserting a disc helps to do this by bringing out the eject button. 4) Double-check that all internal parts of the computer are screwed down and wired up correctly. 5) Re-attach the monitor, keyboard and mains power cables.
- Switch on the monitor and then the computer. The computer should beep and some keyboard lights illuminate if all is well. If not, TURN THE COMPUTER OFF IMMEDIATELY and go through the procedure above, checking as you go, before trying again.
- If no picture appears on the monitor try switching the computer off and then 0n again whilst holding down the DELETE key; this resets configuration memory to use a normal monitor. Consult the User Guide for more information on using different monitors.
- Follow the instructions below and enjoy the increased speed of the computer!

USING THE ARM3 UPGRADE

If you are using RISC OS 3 you do not need our software at all. The operating system will detect the ARM3 Upgrade, but see below about Configuring the ARM3 to work automatically.

The diskette supplied with the ARM3 Upgrade contains the application !Arm3, which must be installed to allow selection of the processor speed. You can do this in one of several ways: the most convenient is to configure your computer so that the application runs automatically as part of the boot sequence when you turn the computer on. We describe how

to do this below.

NOTE: the diskette is usually packed BENEATH the plastic foam in the ARM3 box.

From the Desktop

Enter the desktop and select the disc drive with the Arm3 support disc in it. Double-click on the !Arm3 program and notice that a new icon appears on the right of the icon bar with the legend Arm3. Clicking select on this will change its state, with the faster Cache On state appearing as a hare, while the Cache Off state appears as a tortoise. These sprites appear in the applications' !Sprites file, so you can swop them for others using !Paint if you wish.

From the Supervisor command line

To run the !Arm3 application from the command line put the disc provided in Drive 0 and type in :0.!Arm3. This will set up the application. You can then use the commands *CACHE ON and *CACHE OFF to turn the extra speed on and off from the command line.

You will want to copy the !Arm3 application onto your hard disc, should you have one. If you put it in the root directory then you can run it either by typing in: RUN ADFS::4.$. ! ARM3 or by putting RUN:4.!ARM3 in the !Boot sequence for your computer.

USING THE ARM 3 WITH THE PC EMULATOR

in the PC Emulator vesions 1.30 and later the emulator can be started from the desktop by double clicking on the !PC application. This action will kill off all relocatable modules that have been loaded into RAM by the user, including that which controls the ARM3 cache, so the PC Emulator will not get the benefit of the ARM3. To avoid this the PC Emulator configuration must be changed as follows. Open the !PC application by holding down the Shift key and double clicking on !PC. The configuration file is stored inside the directory (folder) marked GenBoot; open it by double clicking on that icon. Load the file marked !Config into a text editor (such as !Edit). The file consists of a number of 'questions' followed on the next line by an answer: Y or N. The line that says 'Perform RMClear' is usually followed by a 'Y' to tell the system to clear the Relocatable Modules in RAM. Change the line following this question to contain the single letter (CAPITAL) 'N'. Once you have made this change save the file back to where it came from (in !Edit press 'F3' and then 'Return'). Now when the PC Emulator is started it will not clear all the modules.

Note that since the system is no longer removing all the modules that are loaded you may find that the PC Emulator has insufficient memory available to it. If this is a problem you may edit the !Config file again and change the response to the question 'Quit desktop for maximum memory?' to the letter 'Y'. In this case all applications will be stopped and their memory given up, before the PC Emulator starts.

CONFIGURATION OF THE ARM 3 STATE

The !ARM3 application provides a new *CONFIGURE option for the cache. If you enter *CONFIGURE CACHE ON then the computer will start up with the cache on; similarly *CONFIGURE CACHE OFF causes it to start up with the cache 0ff. Entering *CACHE alone causes the computer t0 report the present cache state as On or Off.

TECHNICAL DETAILS

The cache control module provides five SWIs so that programmers can control the cache from their own programs. SWI Cache_Control only uses bit 0 of the registers. If the bit is 0 the cache is switched off; if it is 1 the cache is switched on.

Three further SWIs provide access to the internal registers of the ARM 3. For each of these three calls, R0 contains a data word in which each bit represents a 2MByte chunk of the memory map. Bit 0 represents the memory from &0 to &1FFFFF, and bit 31 represents the chunk from &3E00000 to &3FFFFFF-. A bit set means the chunk is cacheable/ updateable/disruptive; a clear bit means that it is not. The initial settings for these registers are carefully chosen, so do not change them without good cause and knowledge of what you are doing. The SWIs all take two parameters, the current value of the relevant register is logically ANDed with R1 and then EORed with R0. Thus to set the parameter, put a new value in R0 and set R1 to 0. To read the old value put 0 in R0 and -1 in R1. (Hex -1 is &FFFFFFFF.) All these SWIs return the new state in R0.

The SWIs Cache_Cacheable, **Cache_Updateable** and **Cache_Disruptive** determine how the cache behaves during accesses t0 various parts of memory. If memory is marked as cacheable then reads from these locations are cached. I0 space is not cached, as it can change without the processor doing anything. If memory is marked *as* updateable then writes to these locations update the value for that location in the cache if the data has been cached (clearly this should not be the case for Read Only Memory).

If memory is marked as disruptive then any writes to that memory will cause the contents of the cache to be discarded. This is necessary so that when the operating system writes to the memory controller to remap the RAM pages the cache is flushed of any invalid data. It is important to note that misuse of these SWIs can have serious side effects including crashing the machine or making it run very slowly. They should only be used by experienced and capable programmers who need t0 tune the cache to fit a specific application. It is not necessary to use them to take advantage 0f the higher speed offered by the Upgrade.

The final SWI is **Cache_Flush** which simply removes all cached information from the cache; it takes no parameters.

USING THE ARM 3 UPGRADE WITH RiscIX

Versions of Risc/iX numbered 1.13 and later will run if the above instructions are followed. Earlier versions require the use 0f a special version of the ARM3 control software to ensure correct operation with Unix. You will need to install it instead of the Risc OS software; follow these instructions and then double-click on the !ARM3 icon afterwards:

- Hold down a SHIFT key and double-click on the !ARM3 application icon. A series of files will be displayed in a new window.
- Move the pointer to the file called "CacheMdl" and rename it "CmdIROS" and press RETURN.
- Move the pointer t0 the file called "CmdlUnix" and repeat the process above, this time naming it "CacheMdl" instead.
- Close the !ARM3 window and test it out by double-clicking 0n it.
- Risc/iX will now run correctly. To maximise the speed of Risc OS, reverse the renaming process described above (so CmdIROS becomes CacheMdl again).

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