KEEP IT SIMPLE

Chips have become faster, larger and more complex, but at the same time less efficient. Roger Cullis explains how the reduced instruction set microprocessor may solve this problem and looks at Acorn's addition to the fray.

The Reduced Instruction Set Computer (Risc) was born out of the realisation that the current generation of 16- and 32-bit microprocessors do not perform very efficiently. Although their instruction sets are powerful, execution of an op code frequently consumes several clock cycles. This means that the 80286-based IBM PC/ AT, for example, is not much faster than the BBC Micro, which is driven by the humble eight-bit 6502. Added to this, there is a move away from stand-alone computing. Also a fast interrupt response is essential for networking, since characters may be lost if the processor has to complete a multi-cycle instruction before it can service the interrupt request.

Acorn has developed a complete chip set based around a CPU which has only 44 basic instructions that are designed to produce efficient code which executes very quickly. Fabricated in low power consuming CMOS, the Acorn Risc Machine (Arm) has an average execution rate of four million instructions per second (mips) when used with an 8MHz two-phase clock. This makes it two-and-half times as powerful as a Vax 11 / 780 and over eight times more powerful than an IBM PC/ AT.

64MBYTE ADDRESS SPACE

The Risc chip has 32-bit architecture with a 32-bit external data bus and a 26-bit address bus which gives a 64Mbyte uniform address space. The internal construction of the processor is optimised for fast interrupt response and efficient support of high-level languages. The chip set will be manufactured by VLSI Technology of Phoenix, Arizona, which makes the custom-array devices used in current Acorn computers. It will find application in systems that require high computing power or fast response, such a laser-printer controllers, network controllers and graphics work stations.

In comparison, the Motorola 68020, which represents the ultimate development of current processor-design techniques, is produced on a chip that contains 192,000 devices and runs at 2.5mips; the Arm, with higher performance, uses a chip with only 25, 000 devices. This means that the Acorn chip can be produced for 25 percent of the cost of the more complicated CPU — the Arm costs £4,500.

When designing the Risc processor, Acorn chose a 32-bit word length. This represents a compromise between opting for extra computing power and the additional complexity of the encapsulation which would be required to make provision for a 64-bit data bus. The chip has a small optimised instruction set hard wired into a programmable logic array, dedicated registers to handle interrupts and a large memory-toprocessor bandwidth.

The chip uses pipelining so that all parts of the processing and memory system can be used every cycle when executing register-to-register instructions. During each processor cycle, one instruction can control the data path while the system decodes a second instruction for the following cycle and fetches a third from memory. The Arm contains 25 registers which partially overlap to support moving of processing functions from hardware to software. The overlapping removes the need to save the contents of registers and service interrupts quickly.

There are three controller devices for video and audio, memory and I/O which come with the Risc chip. The video controller incorporates a specific section for cursor injection to remove the constraints imposed by the need to generate it by means of software. Another block supervises the generaton of a stereo audio signal. The memory controller supports DMA and has an address translator for virtual-memory systems.

Evaluation systems using the Arm are being produced in two versions. The first is a second processor which follows the established format for use with the BBC Micro. Enclosed in a standard Acorn second-processor box and connected to the base processor by way of a ribbon cable and the Tube interface is a Risc CPU with 512K ROM, I/O and video controllers plus 4Mbyte of dynamic RAM. The BBC Micro based system is already available. At a presentation given to the press it was demonstrated performing fast arithmetic calculations, complex graphics displays and a real-time synthesis of an acoustic guitar. Arm also has mouse and keyboard interfaces.

An IBM PC version will be released soon. It will take the form of a standard card which can be plugged into an IBM PC or PC / AT. It will have 4Mbyte of RAM and offer a similar performance to that of the BBC Micro version.

SOFTWARE SUPPLIED

Both evaluation systems will be supplied with comprehensive documentation and a full set of software tools, including a powerful assembler and an editor, linker, debugger and utilities. The high-level languages are Fortran 77 and a C compiler, which will allow many existing applications packages to be ported across to the new environment. Cambridge Lisp and Prolog X have been provided to meet the needs of the expert-systems market. BBC Basic has also been included to complete the package.

The announcement of Acorn's Risc machine is an indication by Olivetti of its endorsement of Acorn's future role. The Arm gives users the opportunity to gain experience of the next generation of micros, as well as providing a high-performance upgrade path for existing BBC Micros and IBM PCs. However, at this stage the Arm is a solution in search of a problem. But with a comprehensive suite of software tools, a very fast processor and an adequate amount of memory and addressing capability, there is no doubt that many applications will be forthcoming.

THE BACKGROUND TO RISC

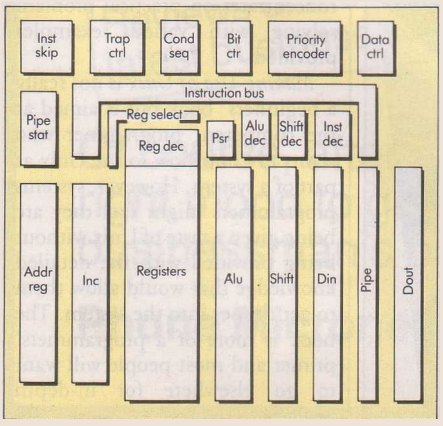
When Intel designed the first microprocessor, it set out on an inexorable path of ever faster, larger and more complex devices. It led from the four-bit 4004, to the eight-bit 8080, the 16-bit 8086 and then to the 32-bit 80386. This progress to greater sophistication is attributable both to improvements in semiconductor technology and to the investment of users in software, which dictated that the instruction set of each new processor should be a super-set of that of its predecessor.

As the chip designers were adding more bells and whistles, it became apparent that the bulk of programming used only a limited proportion of the instructions which were available. As in many other situations, Pareto's Law applied — 20 percent of the instructions accounted for 80 percent of operations. This revelation led to a complete rethink of microprocessor design and gave rise to the Risc concept, which is based on two principles: keep it simple and do it fast.

Risc processors have a small set of regular instructions, of the same size and structure, which execute in a single cycle. This means that the interrupt response is very fast. At the design stage, the inclusion of an extra instruction needs to be justified on both cost and performance. Only the simplest ones, such as add, branch, load and save, satisfy this criterion. The typical layout of the chip is planned to enhance the speed of register transfers. Only load and save operations access memory, and pipelining techniques are employed to minimise delays. Microcode, which involves memory access, is replaced by hard wired logic.

A compact instruction set means that complex functions are assembled from smaller building blocks and consequently programs are longer. Typically, a Risc program may be 30 percent longer than its conventional counterpart and so requires a corresponding increase in memory bandwidth. On the other hand, the same program will occupy one-fifth the number of machine cycles and hence run faster.

The Acorn Risc CPU chip (above) contains 25,000 devices arranged as shown below. Since most activity is based on register transfers the layout is designed to optimise such operations.



WHO USES RISC?

It is generally accepted that the concept of a computer with a small instruction set and simple architecture was first developed by John Cocke, when he was working in the IBM Research Centre on ideas for a fast controller for large telephone switching systems. The principles were further developed at the. University of Berkeley in California, where the acronymn "Risc" was coined.

Other companies making devices ate Inmos with its celebrated T-424 32-bit Transputer and Fairchild with a CMOS device code-named Clipper, which runs at 40MHz. The U.S. defence programme has spawned high-speed devices fabricated in gallium arsenide from McDonnell Douglas and Texas Instruments. Hewlett-Packard and IBM also make devices, but these are reserved for their own use. The company most committed to applications is Hewlett-Packard, which plans to apply the Risc philosophy to its entire product line. IBM caused a few ripples of excitement when it introduced the IBM RT PC personal computer — also known as the 6150 — in January of this year. Based on a 118-instruction CPU, the desk-top machine is attacking the technical work-station market dominated by DEC, Apollo and Sun Microsystems. At the high-performance end, Harris Computer produces the 7mips HCX-7 and Ridge Computers has its 32 / 100 floating-point processor.